# High Density MCM-C Utilizing Tape Dielectric and Photopatterning Processes

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**Abstract**

Two significant extensions of classic ceramic thick film substrate technology have gained increasing acceptance as a means to produce multichip modules. The first extension is low temperature cofire ceramic packaging, which take advantage of the thickness control of a pre-cast insulating tape dielectric combined with the ability to combine several sintering steps into one single firing. The end result is a high density, cost effective substrate/package. The second extension is subtractive formation of conductor and via geometries through the use of photoprocessing and wet chemistry. Well defined 12 micron conductor tracks and fine 50 micron interconnecting vias allow for precise circuit geometries. In combination with high conductivity tracks and low loss and low dielectric constant materials, microwave components may be cost effectively produced where expensive thin film was previously the only technology option possible.

In theory, the marriage of these two technologies would have even greater technical benefit in balancing higher performance with cost per circuit. In practice, this combination has not been practical due to the inability to pattern conductors and vias in high volume production with yet to be cofired tape.

An alternative approach will be described, using the strong points of both dielectric tape and subtractive processing technologies. Simulated MCM-C multilayer substrates using the traditional alumina base substrate, but incorprating tape dielectric layers and photopatterning techniques to produce conductor tracks and components will be presented. Additionally, LTCC modules post-processed with subtractive processed thick film are also discussed. Data will be shown outlining the density capabilities of multilayer substrates constructed that enable complex MCM designs to be cost effectively produced.

Key words: MCM-C, photopatterning, low temperature cofire ceramic, LTCC, tape transfer, buried components.

## Introduction

The requirements for ceramic based multichip module substrates and packages (MCM-C) with respect to materials of construction has gained much attention during the recent past, as materials and substrate suppliers calibrate their efforts to focus on the following generic needs:

| *Need* | *Why* |
|---|---|
| Increasingly high numbers of I/O interconnections | Increasingly complex die |
| Ability to dissipate heat better | Increasingly complex die<br>Higher power requirements |
| Decrease in size/weight | Portability<br>Increase end system functionality |
| Precise conductor and via definition | Increase end system functionality (microwave)<br>Array interconnection (flip chip, BGA, etc.) |
| Low cost | Evolutionary technology adoption MUST cost less to gain acceptance. |

**Table 1: Generic Needs of the Microelectronic Module Designer**

As one can conclude from the above list, substrate and packaging technology continually will be at the mercy of the seemingly endless trend of integration of functions into IC's. Additionally, as the IC's become more complex, the demand for the number of complimentary passive components also rises. The actual substrate surface real estate becomes even more densely populated. The drive to relieve the real estate demands is realized through integrated passive component technology either in the subsequent layers of the multilayer, MCM-C substrate, or to integrate those devices with the IC itself, or both. Aside from the obvious real estate concerns, performance of integrated, multifunction components may be enhanced by imbedding the devices at their optimal location within a multilayer structure.

Several microelectronics packaging technology options exist today, with each technology option possessing a particular set of attributes that make that option a reasonable choice to design an MCM or similar module [1]. The key attributes to be examined in choosing a particular packaging technology are becoming more demanding. Key areas of consideration for the designer are:

- Ability to accommodate high I/O counts and power demands of complex IC's,
- Ability to design RF, analog, and digital - either independently or in combinations,
- Ability to perform at frequencies of 5GHz and greater,
- Compact size and low weight,
- Lowest possible losses to minimize power consumption and hence maximize battery life,
- High reliability,
- Low cost construction to allow for accelerated acceptance of new technologies.

Technologies available to the designer tend to be based on one of three core technologies. These are: MCM-L, using polymer based processes; MCM-D using thin film processes; MCM-C using ceramic substrates, either with a multilayer co-fired ceramic, or a thick film print and fire on ceramic technology.

The apparently low cost polymer technologies offer limited geometries and poor high frequency characteristics. Whilst new materials are becoming available for microwave use, they are generally more expensive than other polymer materials and are still limited in both microwave performance and environmental stability. Hence, although MCM-L technology is enjoying widespread application, it fails to deliver in several applications. The increasing use of build up technologies is aimed at addressing these problems, but the dimensional stability and high RF problems still remain, together with greatly increased complexity of processing and hence cost.

Thin film technology on the other hand offers very high circuit performance. Unfortunately, this is obtained at high cost. The combination of expensive sputtering processes, with high material wastage and expensive polished high purity 99.6% alumina substrates all increase the cost to a point where thin film

technology has a very limited application. Its major relevance being in high speed and microwave circuits.
A general measure of the efficiency of a circuit fabrication technology is the cost per square inch. It is becoming understood that cost per unit area is also a false measure, as an alternative, nominally more expensive technology may allow the same function in a smaller area. This can lead to a lower cost, as well as allowing a smaller overall package with further cost and marketplace benefits

MCM-C offers two contrasting approaches to overcoming these problems. Low temperature co-fired ceramic (LTCC) technology, allows high circuit density by the efficient production of multiple layers and buried components, for applications up to several GHz. Thick film technology provides a solution by means of fine line printing, but cannot offer the small via geometries of LTCC. An advanced thick film technology using novel materials and photo processing to provide very small circuit geometries and outstanding microwave performance is now available, which addresses man of these limitations.

Independently, each technology possesses particular strong points. But combining the strengths of tape and subtractive processing technologies offers even more possibilities for realizing the increasing demands on MCM-C technology. The key features not addressed in this proposed combination, though, are strength and thermal performance. A lesser integration of tape dielectric technology, rather than traditional LTCC technology, may address these needs without sacrificing the overall balance of needs theoretically achieved through integrating cofiring and subtractive processing. Tape transfer or tape on substrate, is a means to apply pre-cast dielectric layers to a base alumina substrate, a substrate typically used in standard thick film constructions. The combination of tape transfer and subtractive processing offers a desirable balance of properties to address a majority of the above stated technical needs

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| | STD THICK FILM | TAPE TRANSFER | SUBTRACTIVE (KQ) | LTCC |
|---|---|---|---|---|
| REDUCED PROCESSING STEPS | ⇓ | ⇔ | ⇔ | ⇑ |
| THERMAL/MECHANICAL INTEGRITY | ⇑ | ⇑ | ⇑ | ⇔ |
| HIGH FREQUENCY | ⇓ | ⇔ | ⇑ | ⇔ |
| INCREASE CIRCUIT DENSITY | ⇓ | ⇔ | ⇑ | ⇑ |
| MFG INFRASTRUCTURE? | ⇑ | ⇑ | ⇔ | ⇑ |

**KEY:** ⇑ = MEETS OR EXCEEDS NEED, ⇔ = MEETS NEED IN SOME CASES, ⇓ = UNMET NEED

**Figure 1: Relative Performance of Advanced Ceramic Technologies Based on Generic Technical Needs** [2]

The integration of dielectric tape technology and subtractive processing will be discussed. A relevant test pattern has been developed to demonstrate the construction of a multilayer, MCM-C substrate. It is the intention of this paper to demonstrate the first order integration of dielectric tape and subtractive processing technology, using well know, established processing techniques and existing infrastructure.

**Background – Materials and Processes**

***Tape Transfer***

Tape transfer is a process developed by the Hughes Corporation in the early 1980's [3]. The inorganic thick film dielectric are similar as the standard paste form, only differing is by the fact that the dielectric is delivered in cast tape form, with or without a carrier. The advantages of using a cast tape as opposed to a screen-printed application are 1) the ability to build an insulating dielectric layer in a multilayer circuit in one step. This replaces screen printing two to three layers to obtain a reliable insulation thickness of the dielectric. 2) Reduction or complete elimination of voiding from printing defects, due to the use of pre-cast tape. Cast tapes are typically inspected in-line during the casting process to determine defects in the surface. 3) Precise control of dielectric thickness. Again, cast tape reduces the inherent variability experienced as a result of screen-printing. This control of thickness allows for more precise control of impedance of the circuit, providing for greater design flexibility. Interconnecting vias are formed mechanically, as is typically done with LTCC. Vias may be formed by punching with a die, laser drilling, or by chemical removal.

The basic process sequence for application of tape transfer to the base substrate follows:


**Figure 2: Basic Tape Transfer Process Flow**

Heraeus p/n CT100 Heratape™ was used for test modules fabricated for this study. The material possess a dielectric constant of aproximately 7 with loss of 0.2%, so structures that operate at 5GHz or below may be suitably designed.

***Low Temperature Cofire Ceramic (LTCC)***

The use of LTCC to fabricate high density reliable MCM-C integral packaging has become standard practice. LTCC shares the same basic benefits of dielectric tape technology with tape transfer. However, LTCC's parallel processing capability facilitates rapid turnaround times with reduced cost on packages with large layer counts. Product employing four mil lines and spaces is being produced on a regular basis and three mil lines and spaces is possible. The use of cavities and thermal via arrays can be used to provide thermal conductivity comparable to that of tape transfer and thick film on alumina. Buried passive components like resistors, inductors, capacitors, and various filter types have been implemented successfully. High frequency inductors are common and buried capacitor dielectrics with K's of 1000 have been tested. Buried resistors may be incorporated to form RC and LRC circuits.

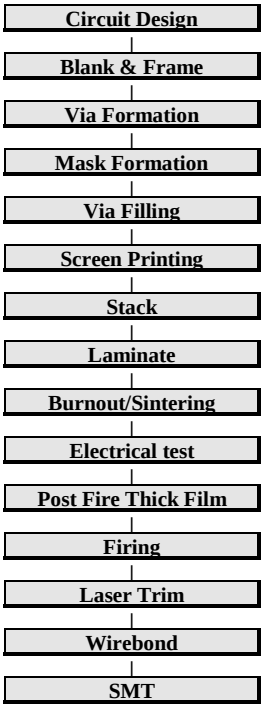



**Figure 3: Basic LTCC Process Flow**

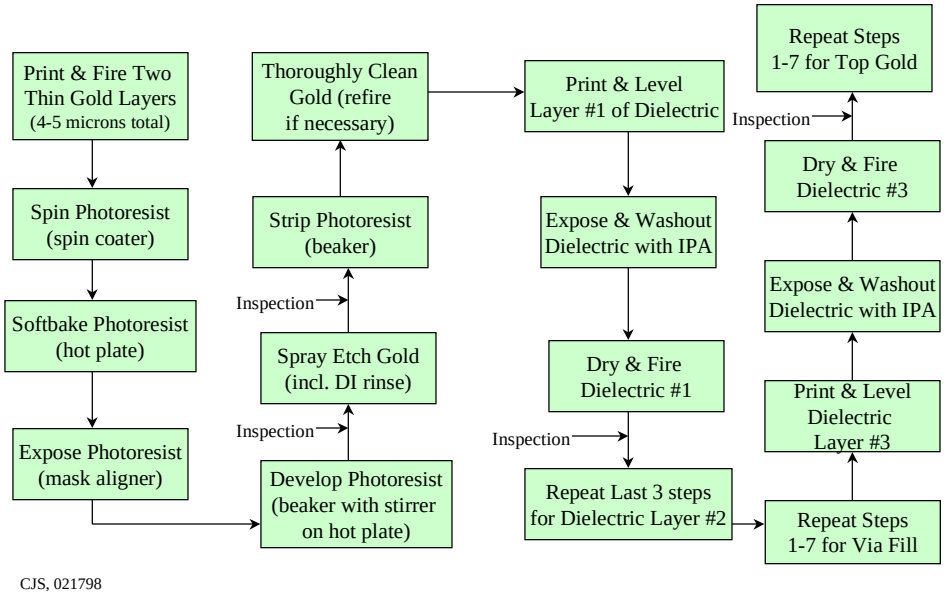



**Figure 4: KQ Subtractive Process**

Heraeus CT700 Low temperature cofire ceramic tape was used to fabriacte modules. The dielectric properties are similar to CT100.

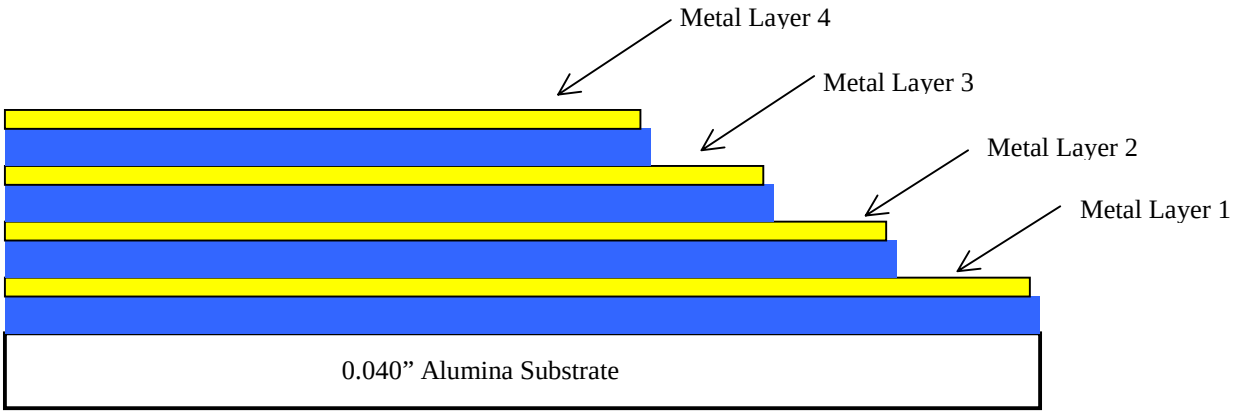
***Subtractive Processing***

The new KQ materials system consists of thick film gold conductors and dielectrics and has been described in detail in previous work [4]. Novel particle sizing in the gold conductor allows the printing and firing of a very smooth gold conductor of high density which in turn allows the application of a photoresist and the patterning of the conductor by a simple etching process. This process provides extremely high resolution lines on 96% alumina as shown in Figure 1. The dielectric materials use a borosilicate glass based technology, which provides low dielectric constant (3.9) and loss (10E-04). The incorporation of a photosensitive vehicle into the dielectric allows the definition of precise via geometries, in the order of 50 microns. The process flow for the technologies is shown below in Figure 4.

Heraeus etchable p/n KQ550 thick film gold was used to fabricate modlues for this study. This material is capable of producing 12 micron lines with +/- 1 micron edge acuity. KQ550 resistivity @ 10 microns is 2.6 milliohm per square.

**Test Vehicle**

The purpose of this demonstration substrate is to prove the feasibility of fabricating a high density interconnected MCM-C using TOS or LTCC with subtractive processing. The cut away demonstration substrate was fabricated using a combination of tape transfer and the Heraeus Cermalloy KQ etching process. This particular substrate design probably represents the most difficult aspects of tape transfer and subtractive processing because of the exposed underlying material during each successive layer addition. Artwork had to be modified to ensure resist material covered underlying metal layers during exposure to protect them during the etch process. This design/process modification would not be required during normal tape transfer or LTCC package fabrication.




Metal Layer 1 – Signal Routing
Metal Layer 2 – Ground Plane
Metal Layer 3 – Spiral Inductors, Wilkinson Dividers, Couplers, Transmission Lines
Metal Layer 4 – Wirebond sites, Chip and Die attach

**Figure 5: Schematic of TOS/KQ Demonstration Circuit**

**Processing & Fabrication**

96% alumina (.040" thick) was used as the base for this structure. It is important that relatively flat, stress free alumina be used to prevent cracking during lamination and firing. Tape to substrate alignment may be accomplished through the use of three point locators and tool pins.

Prior to attaching the first layer of tape to the substrate alignment targets to be used in the glass mask alignment process were screen printed and fired onto the alumina substrate. This thick film ink should be a Pd/Ag type or equivalent to be resistant to the gold etching solution.

Electrical interconnect vias may be formed in the tape using CO2/Eximer laser or mechanical punching techniques. Filling of the vias with conductive material is accomplished by extrusion or screen printing.

The tape was aligned to the alumina substrate, shiny side down positioned on a aluminum lamination plate. A protective sheet of mylar was placed over the top of the tape to prevent sticking during lamination. The lamination plate with substrate was then wrapped in a thin rubber blanket and vacuum sealed in a bag. The substrate was then isostatically laminated for 20 minutes at 2200 psig and 70ºC. After the lamination cycle was completed the substrate was allowed to cool prior to removal from the lamination bag. Care was taken during removal to prevent pulling the tape free of the substrate. Parts were stored in a clean environment prior to and after firing to prevent voiding in the conductors during the etch process. The substrate was fired with a standard one hour 850°C 10 minute flat profile. Thorough cleaning of the substrate after etching and prior to applying the next layer of tape is critical. A solvent wash with bake out was performed. A high temperature refire is recommended.
Figure 5 outlines the tape lamination and gold etch procedure used for each successive layer added to the MCM-C structure.

**Results**

Two basic substrate configurations were designed to demonstrate the use of subtractive processing of thick film conductor with dielectric tape technology. First, a four metal layer tape on substrate test substrate design was devised. This design incorprated signal line widths as low as 30 micron lines and spaces, interconnecting vias, couplers, Wilkinson dividers, transmission lines, buried inductors and resistors. The design simulates the complex geometry demands of next generation MCM-C technology. The second test configuration was the incorporation of post fired and subtractively processed thick film conductors on the surface of an LTCC module. Figures 6 and 7 illustrate the capability of the KQ materials system when processed over the CT100 tape transfer materials.

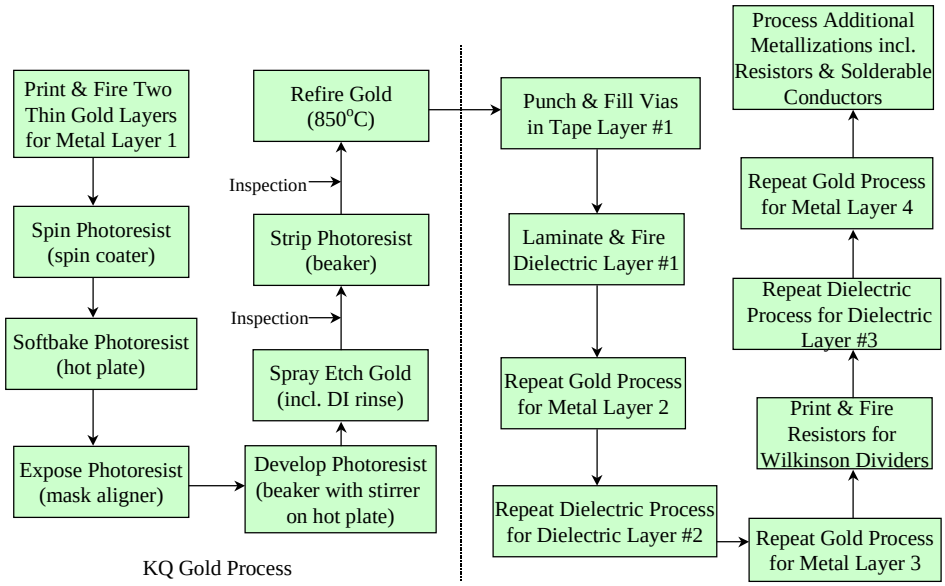



**Figure 5: Manufacturing Process: KQ and Tape Transfer Combination**

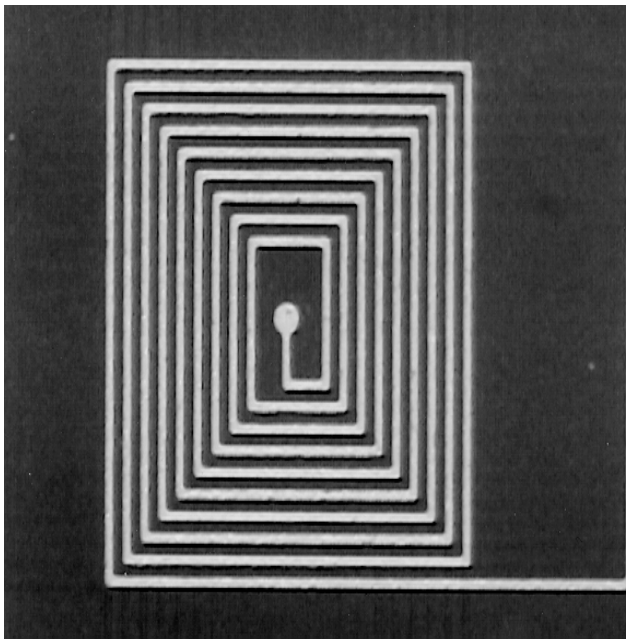


**Figure 6: Spiral Inductor on Tape Transfer**

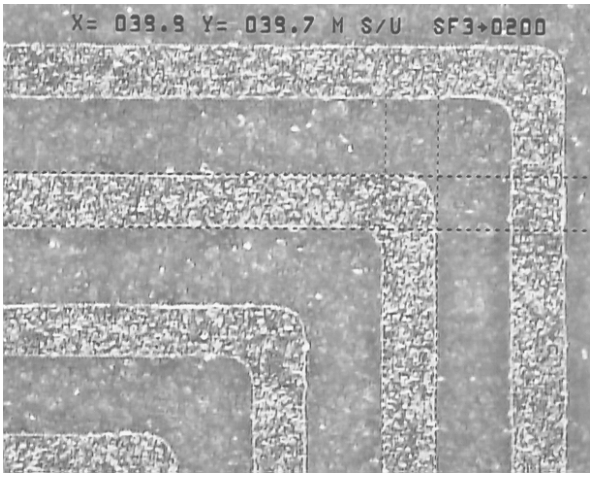



**Figure 7: 30 micron lines on tape transfer, from Spiral Inductor above**

## Conclusions

The first order integration of dielectric tape and subtractive processing has been demonstrated. Simulated MCM-C test substrates were fabricated with integrated passive components suitable for high frequency designs.

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