DESIGN GUIDELINES FOR LTCC

HERALOCK® HL2000 MATERIALS SYSTEM

Preliminary Guideline
Release 1.0
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1. INTRODUCTION

The following documentation has been prepared by Heraeus, Incorporated, Circuit Materials Division, as a guide for both the LTCC foundry and the circuit designer to aid in the application and processing of Heraeus’ LTCC materials. In addition, many LTCC foundries have developed their own set of design guidelines that outline the specific capabilities of that foundry. Where conflicts arise between guidelines published by a specific foundry and guidelines published by Heraeus, the foundry guidelines should be used.

This Heraeus LTCC materials set consists of Heralock® HL2000, as well as a family of conductors in silver, gold, and mixed metal which have been specifically formulated to match the HL2000 tape. This family of materials has been developed to address today’s and emerging market demands for LTCC module design and production. The near zero shrink capability of HL2000 allows for increased ease of use, process simplification, and lower overall cost. HL2000 offers a combination of competitively priced LTCC tape and high performance conductors, which together offer excellent electrical and mechanical performance.

Every effort has been made to make this document as complete as possible. However, errors may occur. If you have questions, please contact the Heraeus Technical Services Department for additional information. In addition, development of new and improved materials is ongoing, and new applications for LTCC are emerging every day. As such, these guidelines should be interpreted as a general guide and not a specific limitation for these materials.

1.1 Glossary of Terms

The terminology used in LTCC can be better understood using diagrams. Figure 1 illustrates a cross-section showing typical via configurations and terminology. Figure 2 shows a top view with cut-aways to illustrate addition features.

Some of the most common terms are defined as follows:

Cavity: a cutout in the tape that extends through several layers, usually larger than a via, and often rectangular in shape.

Foundry: facility that fabricates LTCC circuits.

LTCC: low temperature cofired ceramic.

Via: a hole through the tape layer used for electrical interconnect or thermal transfer between layers.
Figure 1. Cross-section of a six (tape) layer, LTCC package showing common interconnect terminology.

Figure 2. Top view showing feature terminology.
General Design Guidelines for Dimensioning Conductor Traces and Vias:

**Clearance from Substrate Edges**

**Line and Space Dimensions**

Minimum: 3 mil lines and spaces

**Vias**

- Minimum: 5 mils
- Standard: 5-7 mils (6 mils recommended)

**Clearance from Substrate Edges**

- 5 mils Ø
- 15 mils

**Permitted Via Patterns**

- Stacked
- Staggered/Stacked
- Staggered

Recommended via pitch on same layer is 20 mils minimum.

**Circuit Design**

Due to the near zero shrinkage of Heralock® HL2000, this offers many benefits to circuit designers.

Refer to section 3.1, “Design Benefits Specific to Zero Shrink”, for a list of these benefits.
1.2 LTCC Process Flow Diagram

Tape Roll

Blanking & Preconditioning

Via Punching

Via Fill

Conductor Printing

Inspection

Post Processing ← Burnout & Firing ← Lamination ← Stacking

Inspection

Electrical Testing

Singulation

Final Inspection

Circuit Materials Division
Asia cmdinfo@heraeus.com.hk
Europe cmdinfo@heraeus.com
America techservice@4cmd.com

MIT0703.3
1.3 Units of Measure

Unless otherwise specified all units are listed in mils. A mil is .001 inches or 25.4 microns.

2.0 PROCESSING GUIDELINES

2.1 Blanking

Blanking can be done with a razor edge or with a blanking die. Work area should be kept clean and dust free.

2.2 Preconditioning

Recommended preconditioning is 80°C for 10 minutes.

2.3 Punching

Punching is used to create through-holes (vias) for electrical connection, thermal transport, and/or registration. Vias are punched using conventional mechanical punching techniques. Minimum via diameter depends on tape thickness, typically a 1 to 1 aspect ratio should be maintained. Via spacing should be a minimum of 20 mils.

2.4 Printing

2.4.1 Ground Plane Conductor

Ground planes can be printed with conventional screen printers. Vacuum through a porous stone is used to secure the tape during printing. Solid ground planes are recommended. See specific conductor data sheets for processing information.

2.4.2 Routing Conductor

Routing conductor traces are printed using conventional printing techniques. Printing should be done using a 290 - 400 mesh screen. Vacuum through a porous stone is used to secure the tape during printing. See specific data sheets for processing information.

2.4.3 Top Conductor

Top conductors can be printed with the routing conductor silver for non-soldered areas. For areas requiring soldered connections, the solderable top conductor should be used. Lead free solder (95Sn/5Ag) has been found to yield optimal results for aged adhesion. See specific data sheets for processing information.
2.4.4 Via Fill Conductor

Vias can be filled using conventional screen printing. Material should be printed through a stainless steel stencil. Vacuum through a porous stone is used to secure the tape during printing. CL80-8231 should be used for all inner layer via fills and CL80-8290 should be used for the top layer via fill. See specific data sheets for processing information.

2.5 Inspection

Printed layers should be visually inspected prior to lamination.

2.6 Lamination

2.6.1 Registration

Alignment of tape layers can be facilitated by the use of a backing plate with registration pins. Registration holes are punched in the tape during punching step described above.

2.6.2 Pre-lamination

Tacking is recommended to enable final lamination without the use of the registration pins. Removing the registration pins before lamination minimizes the possibility of bag leakage or blistering caused by incomplete evacuation of the bag. Tacking is accomplished by heating the stack to 80°C and applying light pressure to the corners.

2.6.3 Final Lamination

Isostatic lamination is recommended. Care must be taken to completely evacuate bag prior to lamination. Lamination conditions are 1350 psi, at 70°C for 10 minutes.

2.7 Burnout and Firing

Burnout and firing should be done in a box furnace. Recommended firing profile: 3.0°C/minute to 100°C, 2.0°C/minute to 450°C, 8 - 10°C/minute to 865°C, hold for 20 -30 minutes. Cooling rate* is approximately 6 -10°C/minute (furnace cooling rate). Firing must be done on a flat, low contact area setter, such as porous or honey comb. The tape will conform to the setter material.

*Note: As the layer count increases, the burn out ramp rate should be lowered for more efficient burn out.
2.8 Singulation

Singulation can be accomplished in either green or fired state. For green ceramic, the laminate should be heated to 80°C and the razor edge should be heated to 70°C. For fired ceramic, singulation is accomplished by dicing with a diamond saw after firing.

3.0 DESIGN RULES

<table>
<thead>
<tr>
<th>Basic Design Rules</th>
<th>Typical</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Substrate</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Substrate XY dimensions</td>
<td>8”x 8” or above</td>
<td></td>
</tr>
<tr>
<td># of layers</td>
<td>3 to 24</td>
<td>Higher layer count has not yet been tested.</td>
</tr>
<tr>
<td>Fired thickness</td>
<td>10 mils minimum</td>
<td></td>
</tr>
<tr>
<td><strong>Vias</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Green via diameter</td>
<td>Dependent on tape thickness</td>
<td>Via diameter should be ≥ than tape thickness</td>
</tr>
<tr>
<td>Via pitch</td>
<td>20 mils minimum</td>
<td></td>
</tr>
<tr>
<td>Via cover pads</td>
<td>2X via diameter</td>
<td></td>
</tr>
<tr>
<td>Via edge to part edge</td>
<td>15 mils minimum</td>
<td></td>
</tr>
<tr>
<td>Via or pad edge to conductor line</td>
<td>10 mils</td>
<td></td>
</tr>
<tr>
<td><strong>Conductor traces</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Printed line width</td>
<td>4 – 8 mils</td>
<td>3 mils minimum</td>
</tr>
<tr>
<td>Printed line spacing</td>
<td>4 – 8 mils</td>
<td>3 mils minimum</td>
</tr>
<tr>
<td>Line to part edge</td>
<td>10 mils minimum</td>
<td></td>
</tr>
<tr>
<td><strong>Ground Planes</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ground plane coverage</td>
<td>100 %</td>
<td></td>
</tr>
<tr>
<td>Plane to part edge</td>
<td>10 mils</td>
<td></td>
</tr>
<tr>
<td><strong>Cavities</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cavity shape</td>
<td>Rectangular, square, round</td>
<td></td>
</tr>
<tr>
<td>Floor thickness</td>
<td>10 mils minimum (2”x 2”)</td>
<td></td>
</tr>
</tbody>
</table>

*Cavity capability tends to be very foundry specific, depending on forming technique and other processing capabilities. Listed are general guidelines. Foundry specific guidelines should be consulted for cavity specifications.

3.1 Design Benefits Specific to Near-Zero Shrink HL2000

- 1:1 artwork possible
- Very low camber
- Virtually no conductor show through
- Via catch pads may not be necessary
- 100% ground planes possible
- Buried components possible
- Large panel production
### 4.0 MATERIALS SELECTOR

#### LTCC Module Material System

**A:** Solderable Cofireable Silver Based Conductor Overprinted on Silver Conductor  
**B:** Cofireable Gold Wirebondable Gold Conductor  
**C:** Cofireable Silver Internal Signal Layer Conductor  
**D:** LTCC Dielectric tape layers  
**E:** Cofireable Silver Ground Plane  
**F:** Cofireable Solder Mask  
**G:** Solderable Cofireable Silver Conductor Overprinted on Silver Conductor for BGA attach  
**H:** Silver Via Fill  
**I:** Transition Via Fill  
**J:** Top Silver Via Fill

### 4.1 Mixed Metal System

<table>
<thead>
<tr>
<th>Product Code</th>
<th>Product</th>
<th>Description</th>
<th>Resistivity (mΩ/sq)</th>
<th>Thickness (µm)</th>
<th>Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>TC0302 overprinted with TC0305</td>
<td>Cofire Ag</td>
<td>≤ 2</td>
<td>15 - 21</td>
<td>Solderable cofireable silver based conductor</td>
</tr>
<tr>
<td>B</td>
<td>TC7102</td>
<td>Cofire Au</td>
<td>≤ 10</td>
<td>15</td>
<td>Gold wire bondable top conductor</td>
</tr>
<tr>
<td>C</td>
<td>TC0301 TC0302</td>
<td>Cofire Ag</td>
<td>≤ 2</td>
<td>15 - 21</td>
<td>Silver cofireable internal signal layer conductor</td>
</tr>
<tr>
<td>D</td>
<td>HL2000 5.3 (CL91-8242)</td>
<td>LTCC Tape</td>
<td></td>
<td></td>
<td>LTCC dielectric tape</td>
</tr>
<tr>
<td>E</td>
<td>TC0302</td>
<td>Cofire Ag</td>
<td>≤ 2</td>
<td>15 - 21</td>
<td>Silver ground plane</td>
</tr>
<tr>
<td>F</td>
<td>TO2001</td>
<td>Cofireable Solder Mask</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>G</td>
<td>TC0302 overprinted with TC0305</td>
<td>Solderable silver based conductor for BGA attach</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>H</td>
<td>TC0303</td>
<td>Ag via fill</td>
<td></td>
<td></td>
<td>Inner layer via fill</td>
</tr>
<tr>
<td>I</td>
<td>TC7406</td>
<td>Ag/Pd via fill</td>
<td></td>
<td></td>
<td>Transition via fill</td>
</tr>
<tr>
<td>J</td>
<td>TC0304</td>
<td>Ag via fill</td>
<td></td>
<td></td>
<td>Top layer via fill</td>
</tr>
</tbody>
</table>
## 5.0 CERAMIC MATERIALS PROPERTIES

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>5.1 Electrical</strong></td>
<td></td>
</tr>
<tr>
<td>Relative Permittivity</td>
<td>7.3</td>
</tr>
<tr>
<td>(K @2.5 GHz)</td>
<td></td>
</tr>
<tr>
<td>Loss Tangent</td>
<td>&lt; 0.0026</td>
</tr>
<tr>
<td>(@2.5 GHz)</td>
<td></td>
</tr>
<tr>
<td>Breakdown Voltage</td>
<td>&gt; 3000 V/layer</td>
</tr>
<tr>
<td>Insulation Resistance</td>
<td>&gt; $10^{13}$Ωcm</td>
</tr>
<tr>
<td><strong>5.2 Mechanical</strong></td>
<td></td>
</tr>
<tr>
<td>Fired Density</td>
<td>2.9 g/cm$^3$</td>
</tr>
<tr>
<td>Flexural Strength</td>
<td>&gt; 200 Mpa (ASTM # F394-78)</td>
</tr>
<tr>
<td>Surface Roughness</td>
<td>&lt; 0.7 µm</td>
</tr>
<tr>
<td>Camber*</td>
<td>&lt; 1 mil/inch on a 2&quot; x 2&quot; part</td>
</tr>
<tr>
<td><strong>5.3 Thermal</strong></td>
<td></td>
</tr>
<tr>
<td>Coefficient of Expansion</td>
<td>6.1 ppm/°C (20 - 300°C)</td>
</tr>
<tr>
<td>Thermal Conductivity</td>
<td>3.0 W/mK</td>
</tr>
<tr>
<td><strong>5.4 Tape Properties</strong></td>
<td></td>
</tr>
<tr>
<td>Green Density</td>
<td>2.45 g/cm$^3$</td>
</tr>
<tr>
<td>Tensile Strength</td>
<td>240 psi</td>
</tr>
<tr>
<td>Green Thickness (mils)</td>
<td>5.25</td>
</tr>
<tr>
<td>Fired Thickness (mils)</td>
<td>3.5 to 3.75</td>
</tr>
<tr>
<td>Shrinkage XY**</td>
<td>0.16 to 0.24%</td>
</tr>
<tr>
<td>Total Z Shrinkage</td>
<td>32%</td>
</tr>
<tr>
<td>Color</td>
<td>Light blue</td>
</tr>
</tbody>
</table>

* With reasonably balanced structure.

** Shrinkage may vary depending on process and design conditions.
6.0 CAPACITORS

Capacitors can be incorporated into LTCC structures in several different ways. As discrete components, chip capacitors can be surface mounted to the substrate or mounted in preformed cavities.

As embedded devices, simple parallel plate capacitors can be manufactured into the structure by adding large areas of conductor material aligned on successive layers of tape. Typically one of the electrode pads is slightly larger to offset alignment effects. Capacitance is governed by the overlap area, the dielectric thickness, and the relative permittivity according to the relationship:

\[ C = \varepsilon_r \frac{A}{d} \]

\( \varepsilon_r \): relative permittivity
\( A \): overlap area
\( d \): dielectric thickness

In practice, overlap area is limited to about .25 inches square, and adjacent capacitors must be separated by a distance equivalent to the width of the plate. Capacitors fabricated in this manner are somewhat restricted to low capacitance values due to the relatively low dielectric constant of the dielectric, the relatively thick tape, and the limited print area.

Alternately, much higher capacitance value capacitors can be formed by successively printing a conductor pad, then a dielectric material, then another conductor pad. This technique can accommodate much thinner dielectric layers and much higher dielectric constant materials. These materials are currently in development.

A third option is to incorporate planar, interdigitated capacitors. In this configuration, the capacitor is formed by printing alternating fingers of conductor material that are coupled by a terminal strip on either side, see Figure 3. This technique is commonly used at microwave frequencies in part because high Q values are attained. Simulator models are used to determine optimum design.

In all cases it is important to maintain other general design rules.
7.0 INDUCTORS

Inductors are typically incorporated into LTCC packages as conductor lines printed in a coiled configuration. Figure 4 shows a square spiral inductor design. These coils can be connected through vias in successive layers to create higher value inductors. An expression for the inductance of a planar spiral inductor was developed by Wheeler:

\[ L = \frac{a^2 \cdot n^2}{(8a + 11c) \cdot 25.4} \]

where \( a \) is the mean radius of the spiral, \( n \) is the number of turns, and \( c \) is the outer diameter minus the inner diameter as defined by the figure – all dimensions in cm, 1 inch = 2.54 cm. This formula was derived for circular coils but also gives a useful estimation for square spirals. In the actual design of a planar spiral inductor the available circuit area and the inductance value required would have a significant impact on the design, but there are also a number of additional variables that will affect the performance of the inductor.

One of the most important parameters of an inductor is Q factor. For optimum Q factor, the following points need to be considered:

1. A circular planar spiral gives around 20% increase in Q factor over a square one of equivalent linear dimensions.

2. The highest conductivity material should be used – this normally means either pure silver or gold conductor tracks.

3. Print thickness should be as high as possible compatible with the material, processing and geometrical requirements. At microwave frequencies however,
skin depth plays a major role and there is little to be gained from a conductor in excess of 3 times the skin depth. At 2 GHz the skin depth in silver is 1.45 micron and in gold 1.76 micron.

4. Conductor width should be as great as possible.

5. Winding turns into the middle of the inductor gives little increase in inductance, but significant increase in loss. Hence there is an optimum for the ratio of outer diameter (d1) to inner diameter (d2). A figure of between 3 and 4 has been shown to provide this optimum.

Figure 4. A typical planar spiral inductor.

The descriptions and engineering data shown here have been compiled by Heraeus using commonly-accepted procedures, in conjunction with modern testing equipment, and have been compiled as according to the latest factual knowledge in our possession. The information was up-to-date on the date this document was printed (latest versions can always be supplied upon request). Although the data is considered accurate, we cannot guarantee accuracy, the results obtained from its use, or any patent infringement resulting from its use (unless this is contractually and explicitly agreed in writing, in advance). The data is supplied on the condition that the user shall conduct tests to determine materials suitability for a particular application.