Heraeus

Technical Information

DESIGN GUIDELINES FOR LTCC

HERALOCK® HL2000 MATERIALS SYSTEM

Preliminary Guideline
Release 1.0

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1. INTRODUCTION

The following documentation has been prepared by Heraeus, Incorporated, Circuit Materials Division, as a guide for both the LTCC foundry and the circuit designer to aid in the application and processing of Heraeus' LTCC materials. In addition, many LTCC foundries have developed their own set of design guidelines that outline the specific capabilities of that foundry. Where conflicts arise between guidelines published by a specific foundry and guidelines published by Heraeus, the foundry guidelines should be used.

This Heraeus LTCC materials set consists of Heralock® HL2000, as well as a family of conductors in silver, gold, and mixed metal which have been specifically formulated to match the HL2000 tape. This family of materials has been developed to address today's and emerging market demands for LTCC module design and production. The near zero shrink capability of HL2000 allows for increased ease of use, process simplification, and lower overall cost. HL2000 offers a combination of competitively priced LTCC tape and high performance conductors, which together offer excellent electrical and mechanical performance.

Every effort has been made to make this document as complete as possible. However, errors may occur. If you have questions, please contact the Heraeus Technical Services Department for additional information. In addition, development of new and improved materials is ongoing, and new applications for LTCC are emerging every day. As such, these guidelines should be interpreted as a general guide and not a specific limitation for these materials.

1.1 Glossary of Terms

The terminology used in LTCC can be better understood using diagrams. Figure 1 illustrates a cross-section showing typical via configurations and terminology. Figure 2 shows a top view with cut-aways to illustrate addition features.
Some of the most common terms are defined as follows:

Cavity: a cutout in the tape that extends through several layers, usually larger than a via, and often rectangular in shape

Foundry: facility that fabricates LTCC circuits.

LTCC: low temperature cofired ceramic.

Via: a hole through the tape layer used for electrical interconnect or thermal transfer between layers.

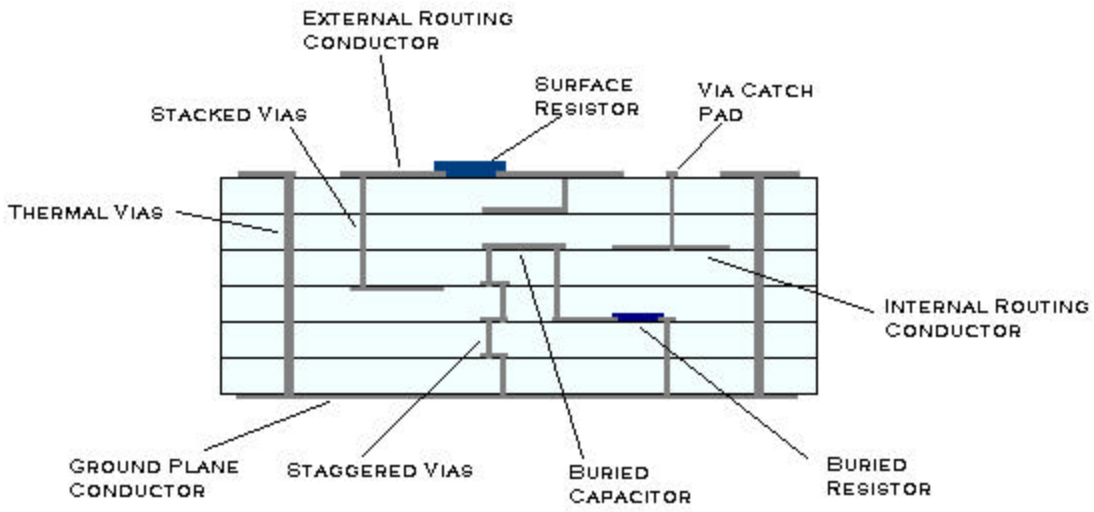

Figure 1. Cross-section of a six (tape) layer, LTCC package showing common interconnect terminology.

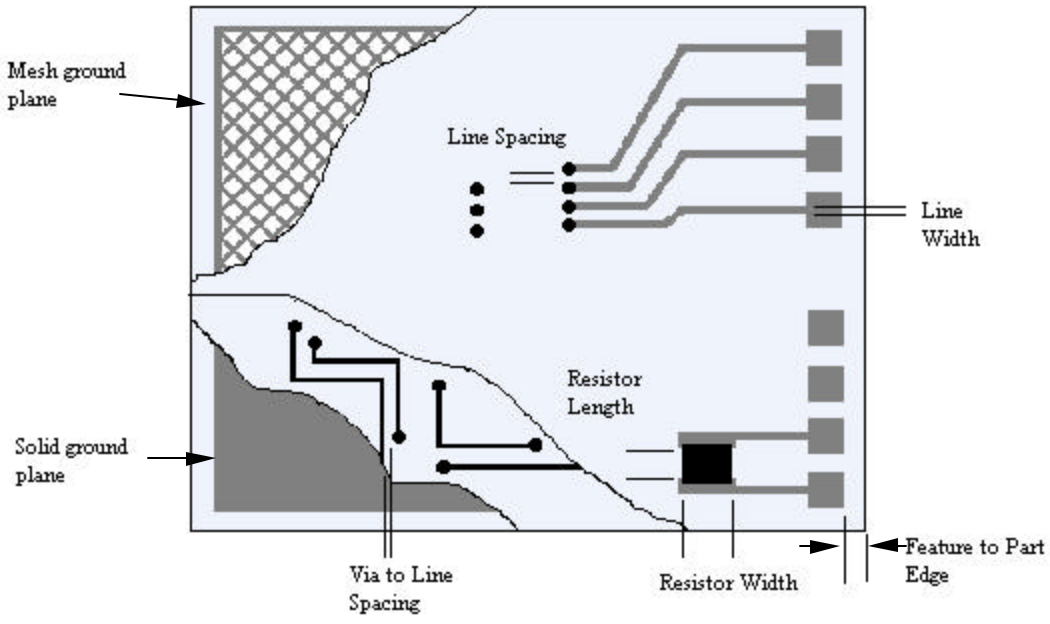

Figure 2. Top view showing feature terminology.

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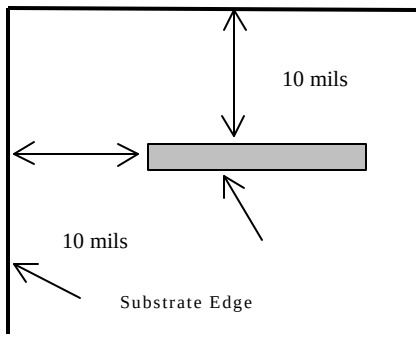
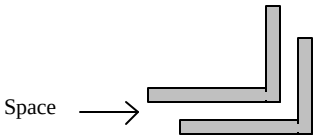
General Design Guidelines for Dimensioning Conductor Traces and Vias:

Clearance from Substrate Edges

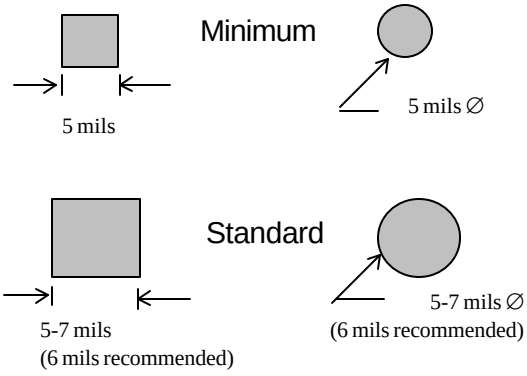


Line and Space Dimensions

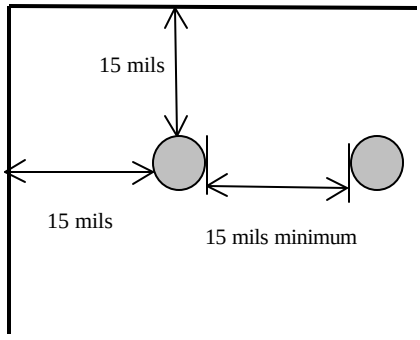


Minimum: 3 mil lines and spaces

Vias

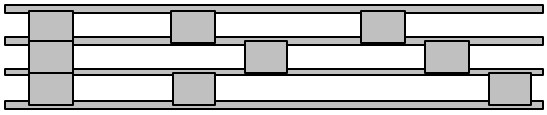


Clearance from Substrate Edges



Permitted Via Patterns

Stacked Staggered/Stacked Staggered



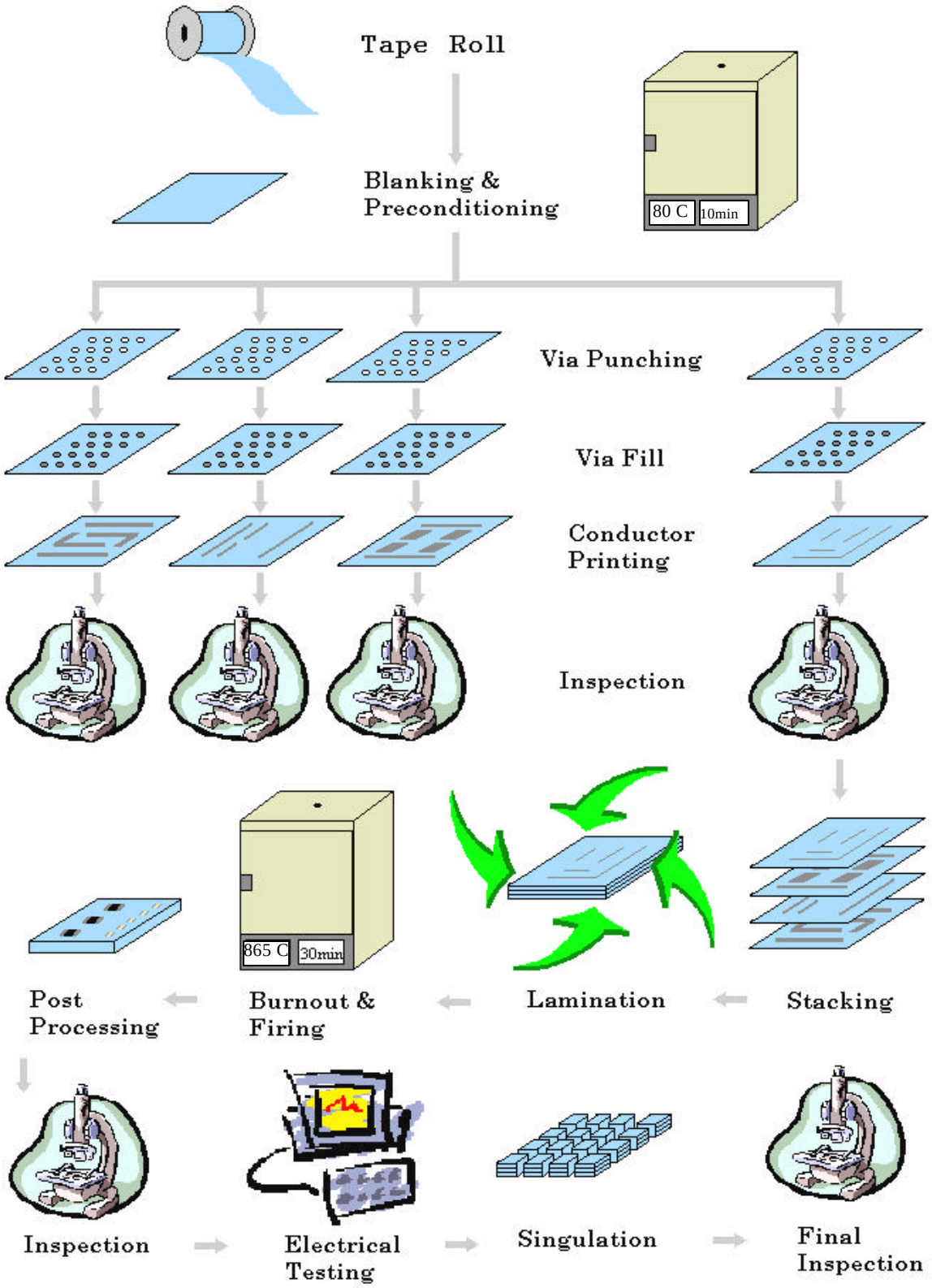
Recommended via pitch on same layer is 20 mils minimum.

Circuit Design

Due to the near zero shrinkage of Heralock® HL2000, this offers many benefits to circuit designers.

Refer to section 3.1, “Design Benefits Specific to Zero Shrink”, for a list of these benefits.

1.2 LTCC Process Flow Diagram



1.3 Units of Measure

Unless other wise specified all units are listed in mils. A mil is .001 inches or 25.4 microns.

2.0 PROCESSING GUIDELINES

2.1 Blanking

Blanking can be done with a razor edge or with a blanking die. Work area should be kept clean and dust free.

2.2 Preconditioning

Recommended preconditioning is 80°C for 10 minutes.

2.3 Punching

Punching is used to create through-holes (vias) for electrical connection, thermal transport, and/or registration. Vias are punched using conventional mechanical punching techniques. Minimum via diameter depends on tape thickness, typically a 1 to 1 aspect ratio should be maintained. Via spacing should be a minimum of 20 mils.

2.4 Printing

2.4.1 Ground Plane Conductor

Ground planes can be printed with conventional screen printers. Vacuum through a porous stone is used to secure the tape during printing. Solid ground planes are recommended. See specific conductor data sheets for processing information.

2.4.2 Routing Conductor

Routing conductor traces are printed using conventional printing techniques. Printing should be done using a 290 - 400 mesh screen. Vacuum through a porous stone is used to secure the tape during printing. See specific data sheets for processing information.

2.4.3 Top Conductor

Top conductors can be printed with the routing conductor silver for non-soldered areas. For areas requiring soldered connections, the solderable top conductor should be used. Lead free solder (95Sn/5Ag) has been found to yield optimal results for aged adhesion. See specific data sheets for processing information.

2.4.4 Via Fill Conductor

Vias can be filled using conventional screen printing. Material should be printed through a stainless steel stencil. Vacuum through a porous stone is used to secure the tape during printing. CL80-8231 should be used for all inner layer via fills and CL80-8290 should be used for the top layer via fill. See specific data sheets for processing information.

2.5 Inspection

Printed layers should be visually inspected prior to lamination.

2.6 Lamination

2.6.1 Registration

Alignment of tape layers can be facilitated by the use of a backing plate with registration pins. Registration holes are punched in the tape during punching step described above.

2.6.2 Pre-lamination

Tacking is recommended to enable final lamination without the use of the registration pins. Removing the registration pins before lamination minimizes the possibility of bag leakage or blistering caused by incomplete evacuation of the bag. Tacking is accomplished by heating the stack to 80°C and applying light pressure to the corners.

2.6.3 Final Lamination

Isostatic lamination is recommended. Care must be taken to completely evacuate bag prior to lamination. Lamination conditions are 1350 psi, at 70°C for 10 minutes.

2.7 Burnout and Firing

Burnout and firing should be done in a box furnace. Recommended firing profile: 3.0°C/minute to 100°C, 2.0°C/minute to 450°C, 8 - 10°C/minute to 865°C, hold for 20 -30 minutes. Cooling rate* is approximately 6 -10°C/minute (furnace cooling rate). Firing must be done on a flat, low contact area setter, such as porous or honey comb. The tape will conform to the setter material.

*Note: As the layer count increases, the burn out ramp rate should be lowered for more efficient burn out.

2.8 Singulation

Singulation can be accomplished in either green or fired state. For green ceramic, the laminate should be heated to 80°C and the razor edge should be heated to 70°C. For fired ceramic, singulation is accomplished by dicing with a diamond saw after firing.

3.0 DESIGN RULES

Basic Design Rules	Typical	Comments
Substrate		
Substrate XY dimensions	8"x 8" or above	
# of layers	3 to 24	Higher layer count has not yet been tested.
Fired thickness	10 mils minimum	
Vias		
Green via diameter	Dependent on tape thickness	Via diameter should be ≥ than tape thickness
Via pitch	20 mils minimum	
Via cover pads	2X via diameter	
Via edge to part edge	15 mils minimum	
Via or pad edge to conductor line	10 mils	
Conductor traces		
Printed line width	4 – 8 mils	3 mils minimum
Printed line spacing	4 – 8 mils	3 mils minimum
Line to part edge	10 mils minimum	
Ground Planes		
Ground plane coverage	100 %	
Plane to part edge	10 mils	
Cavities*		
Cavity shape	Rectangular, square, round	
Floor thickness	10 mils minimum (2"x 2")	

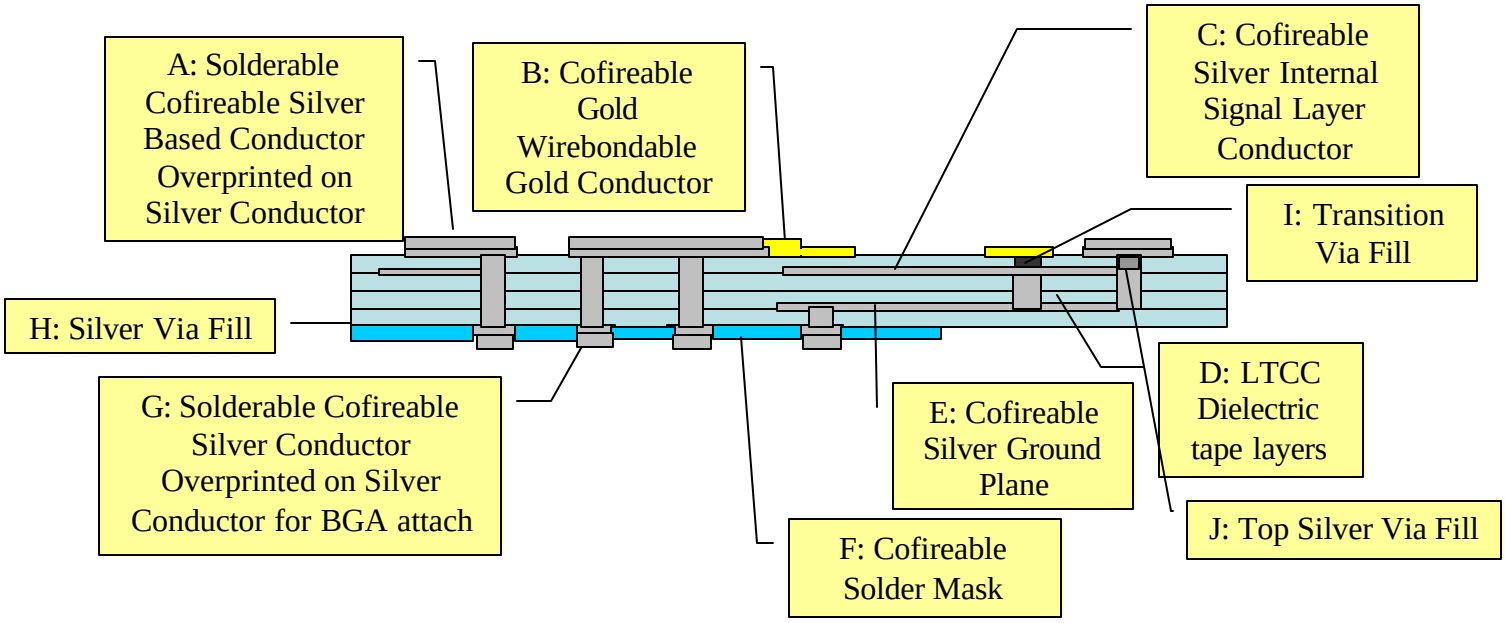
*Cavity capability tends to be very foundry specific, depending on forming technique and other processing capabilities. Listed are general guidelines. Foundry specific guidelines should be consulted for cavity specifications.

3.1 Design Benefits Specific to Near-Zero Shrink HL2000

- 1:1 artwork possible
- Very low camber
- Virtually no conductor show through
- Via catch pads may not be necessary
- 100% ground planes possible
- Buried components possible
- Large panel production

4.0 MATERIALS SELECTOR

LTCC Module Material System



4.1 Mixed Metal System

Product Code	Product	Description	Resistivity (mΩ/sq)	Thickness (µm)	Application
A	TC0302 overprinted with TC0305	Cofire Ag	≤ 2	15 - 21	Solderable cofireable silver based conductor
B	TC7102	Cofire Au	≤ 10	15	Gold wire bondable top conductor
C	TC0301 TC0302	Cofire Ag	≤ 2	15 - 21	Silver cofireable internal signal layer conductor
D	HL2000 5.3 (CL91-8242)	LTCC Tape			LTCC dielectric tape
E	TC0302	Cofire Ag	≤ 2	15 - 21	Silver ground plane
F	TO2001	Cofireable Solder Mask			
G	TC0302 overprinted with TC0305				Solderable cofireable silver based conductor for BGA attach
H	TC0303	Ag via fill			Inner layer via fill
I	TC7406	Ag/Pd via fill			Transition via fill
J	TC0304	Ag via fill			Top layer via fill

5.0 CERAMIC MATERIALS PROPERTIES

Property	Value
5.1 Electrical	
Relative Permittivity (K @2.5 GHz)	7.3
Loss Tangent (@2.5 GHz)	< 0.0026
Breakdown Voltage	> 3000 V/layer
Insulation Resistance	$>10^{13}\Omega$cm
5.2 Mechanical	
Fired Density	2.9 g/cm^3
Flexural Strength	> 200 Mpa (ASTM # F394-78)
Surface Roughness	<0.7µm
Camber*	< 1 mil/inch on a 2" x 2" part
5.3 Thermal	
Coefficient of Expansion	6.1 ppm/°C (20 - 300°C)
Thermal Conductivity	3.0 W/mK
5.4 Tape Properties	
Green Density	2.45 g/cm^3
Tensile Strength	240 psi
Green Thickness (mils)	5.25
Fired Thickness (mils)	3.5 to 3.75
Shrinkage XY**	0.16 to 0.24%
Total Z Shrinkage	32%
Color	Light blue

* With reasonably balanced structure.
** Shrinkage may vary depending on process and design conditions.

6.0 CAPACITORS

Capacitors can be incorporated into LTCC structures in several different ways. As discrete components, chip capacitors can be surface mounted to the substrate or mounted in preformed cavities.

As embedded devices, simple parallel plate capacitors can be manufactured into the structure by adding large areas of conductor material aligned on successive layers of tape. Typically one of the electrode pads is slightly larger to offset alignment effects. Capacitance is governed by the overlap area, the dielectric thickness, and the relative permittivity according to the relationship:

$C = \varepsilon_r A/d$ ε_r: relative permittivity
A: overlap area
d: dielectric thickness

In practice, overlap area is limited to about .25 inches square, and adjacent capacitors must be separated by a distance equivalent to the width of the plate. Capacitors fabricated in this manner are somewhat restricted to low capacitance values due to the relatively low dielectric constant of the dielectric, the relatively thick tape, and the limited print area.

Alternately, much higher capacitance value capacitors can be formed by successively printing a conductor pad, then a dielectric material, then another conductor pad. This technique can accommodate much thinner dielectric layers and much higher dielectric constant materials. These materials are currently in development.

A third option is to incorporate planar, interdigitated capacitors. In this configuration, the capacitor is formed by printing alternating fingers of conductor material that are coupled by a terminal strip on either side, see Figure 3. This technique is commonly used at microwave frequencies in part because high Q values are attained. Simulator models are used to determine optimum design.

In all cases it is important to maintain other general design rules.

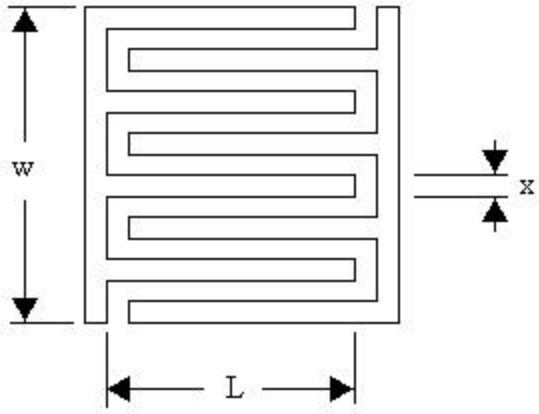


Figure 3. Basic design of an interdigitated capacitor.

7.0 INDUCTORS

Inductors are typically incorporated into LTCC packages as conductor lines printed in a coiled configuration. Figure 4 shows a square spiral inductor design. These coils can be connected through vias in successive layers to create higher value inductors. An expression for the inductance of a planar spiral inductor was developed by Wheeler:

$$L = \frac{a^2 n^2}{(8a + 11c)25.4}$$

where *a* is the mean radius of the spiral, *n* is the number of turns, and *c* is the outer diameter minus the inner diameter as defined by the figure – all dimensions in cm, 1 inch = 2.54 cm. This formula was derived for circular coils but also gives a useful estimation for square spirals. In the actual design of a planar spiral inductor the available circuit area and the inductance value required would have a significant impact on the design, but there are also a number of additional variables that will affect the performance of the inductor.

One of the most important parameters of an inductor is Q factor. For optimum Q factor, the following the following points need to be considered:-

1. A circular planar spiral gives around 20% increase in Q factor over a square one of equivalent linear dimensions.

2. The highest conductivity material should be used – this normally means either pure silver or gold conductor tracks.

3. Print thickness should be as high as possible compatible with the material, processing and geometrical requirements. At microwave frequencies however,

skin depth plays a major role and there is little to be gained from a conductor in excess of 3 times the skin depth. At 2 GHz the skin depth in silver is 1.45 micron and in gold 1.76 micron.

4. Conductor width should be as great as possible.

5. Winding turns into the middle of the inductor gives little increase in inductance, but significant increase in loss. Hence there is an optimum for the ratio of outer diameter (d1) to inner diameter (d2). A figure of between 3 and 4 has been shown to provide this optimum.

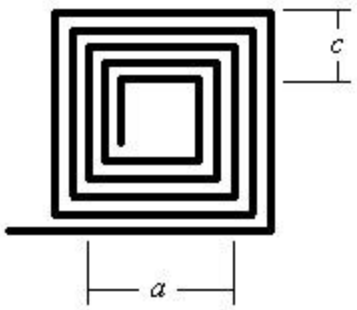


Figure 4. A typical planar spiral inductor.