Microwave Module Design with HeraLock™ HL2000 LTCC

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Abstract

The free-sintered LTCC manufacturing process is a cost-effective approach for building complex electronic modules, especially when good RF performance is needed. The x-y shrinkage and the shrinkage variation that occurs during the firing of standard LTCC is a limitation of this technology for large format manufacturing processes and can cause problems with precision microwave structures. Although several techniques for controlling the x-y shrinkage with constrained sintering have been developed, these additional processes tend to complicate the manufacturing process.

HeraLock™ 2000 LTCC tape (patent pending) is formulated to yield the benefits of constrained sintering techniques with a free-sintered process. While standard LTCC has x-y shrinkage similar to the shrinkage in the z-axis, free-sintered HeraLock™ 2000 densifies primarily in the z-axis, leaving near-zero shrinkage in the x and y directions. The HeraLock™ 2000 tape is lead-free and cadmium-free with fired properties appropriate for microwave devices requiring low-loss at frequencies up to at least 6 GHz as well as automotive and general-purpose packaging applications.

The effect of various firing profile variations on the shrinkage of HL2000 is discussed. Mobile residual glass affects LTCC tapes to varying degrees; these effects will be discussed in the context of conductor and post-fired resistor performance. An overview of microwave material testing with the HL2000 material set will also be shown. The benefits of the HeraLock™ 2000 material system for existing applications as well as for entirely new module designs will be described. The self-constrained tape has unique advantages for building cavity structures and integrating passive components. New fiber optic packaging structures are also enabled.

Key words: LTCC, constrained sintering, RF materials, cavity structures, microwave, embedded passives

Introduction

HeraLock™ HL2000 is a self-constrained low-temperature cofired ceramic (LTCC) tape. The use of a self-constrained tape gives benefits both for the simplicity of the manufacturing process and for the variety of new design applications. Self-constraint gives HeraLock™ tape x-y shrinkage control better than sacrificial layer constraint in a free-sintered process. This eliminates the cost associated with adding and removing sacrificial materials and retains compatibility with cofired solderable or wire-bondable top conductors.

The shrinkage control afforded by self-constraint is an obvious advantage; a more subtle benefit is related to the control of effects related to mobile residual glass on the fired tape surface. In an unconstrained LTCC module, minimizing the camber related to conductor coverage is an important consideration. An increased content of free glass significantly reduces tape camber, but it can have a negative affect on conductor solderability. Because the self-constraint gives Heralock™ HL2000 outstanding resistance to camber, the tape was formulated to yield a nearly dry (glass-free) ceramic surface after firing.

Many processes for achieving constrained sintering have been implemented to realize the important advantages of dimensional control. Usually these techniques complicate the manufacturing process and limit design flexibility. For example, sacrificial constraint methods involve adding more layers to the tape structure in a second lamination step; after firing these sacrificial layers must be removed sufficiently to ensure that the surface conductors are solderable; wirebond pads must then be post-fired onto the surface to avoid contamination by the sacrificial layer material. In addition, the sacrificial layer process is usually incompatible with cavity structures. In contrast, HeraLock™ enabled tape simplifies the process of forming precise cavity structures. Low x-y shrinkage also enables firing the tape with embedded passive devices such as ferrite transformers, chip capacitors or buried optical fibers.

The Benefits of HL2000 for Microwave Modules Design

This paper will discuss several aspects of HeraLock™ HL2000 that represent significant advantages for designers of microwave circuits. These benefits include:

- Precise control of spacing in and between layers.
- Large format size compatibility
- Precision cavity structures.
- Embedded passive structures.
- Highly solderable, camber-free conductors
- 100% coverage ground planes
- Low dielectric loss at up to at least 6 GHz.

Conductor Shrinkage Measurement

It is important the control of x-y shrinkage of the HL2000 dielectric carries over to conductors printed on the tape. Control of dimensions between layers is necessary for devices like the broadside coupler (Figure 1); minimizing the shrinkage of co-fired conductors is critical to ensuring reproducible performance of the RF structures.

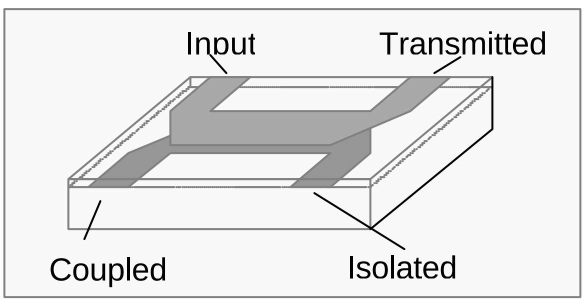

Figure 1: Broadside coupler. The structure requires precise alignment between two metal layers.

A test structure to evaluate conductor shrinkage is drawn in Figure 2. It consists of a conductor snake pattern that has been partly buried by a cover strip of tape. The X-ray of a fired part made with HL2000 and a silver routing conductor is shown in Figure 3. Before firing, a strip was cut off and left in its green state. The test part shows a slight shrinkage of the surface conductor (measured at about 4% of the line-width) and no measurable shrinkage of the buried conductors, relative to the green conductor runners. In addition, there is virtually no shrinkage of the fired HL2000 structure relative to the remaining green strip.

Dimensional Variation & Control

A key benefit of HeraLock™ HL2000 is that its self-constraint enables large format processes because it reduces the dimensional variation occurring during firing. The positional tolerance (i.e., the maximum deviation from nominal position) of a patterned feature due to shrinkage variation is calculated as size multiplied by variation. Figure 4 shows a graph of the expected tolerance of position for three processes: standard free-sintered LTCC, DP951 with sacrificial constraint layers, and free-sintered Heralock™ HL2000. To calculate this tolerance, the total shrinkage variation for standard LTCC was taken to be +/- 0.2% regardless of format size. For both HL2000 and constrained sintered DP951, the total shrinkage variation was calculated as +/- 3σ, where the standard deviation of the shrinkage is measured over a length of five inches (127 mm) [0.04% for DP951 with sacrificial layers [2], and 0.014% for HL2000]. Figure 4 shows that for a given format size a much smaller variation of feature position will be observed for HL2000 than for the other two processes.

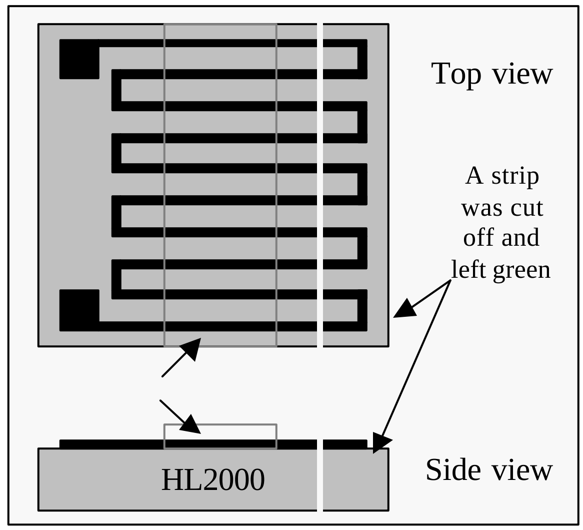

Figure 2: Test structure to evaluate surface and buried conductor shrinkage during firing.

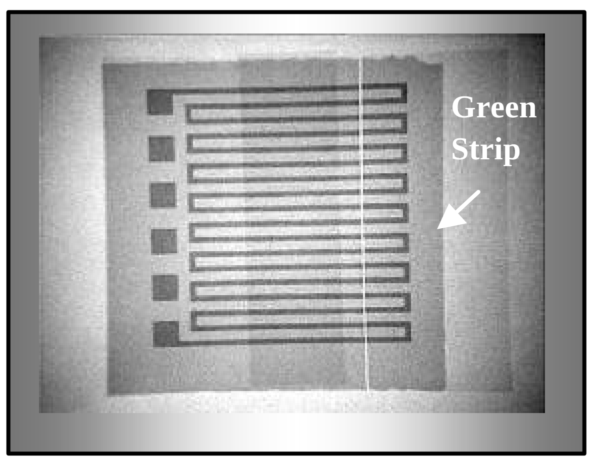

Figure 3: X-ray of test structure.

Cavity Structures

Because the HeraLock™ HL2000 tape maintains its x-y geometry through firing, cavities cut into the tape show minimal distortion. As an example, Figure 5 shows a module made from HL2000 that has a deep slot cavity. The laminate has been cut in half before one of the sides was been fired. After firing, only the change in color distinguishes the two halves.

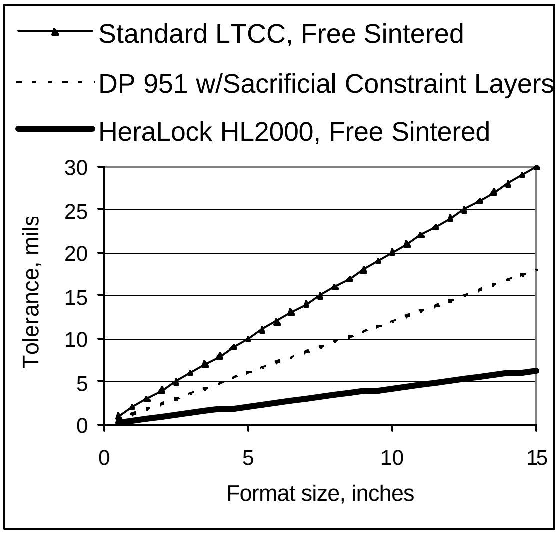

Figure 4: Positional tolerance plotted versus LTCC format size for three different processes.

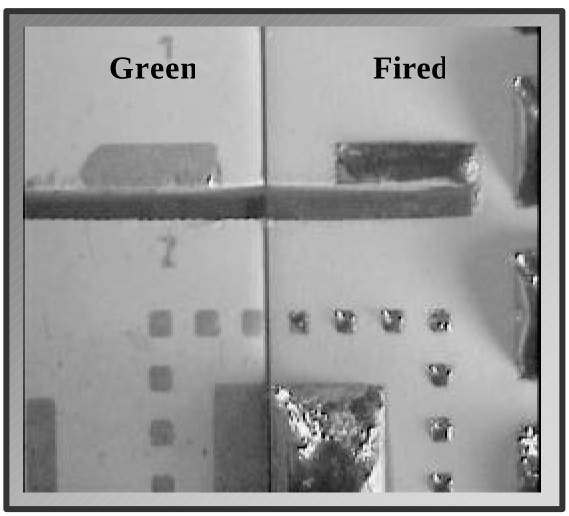

Figure 5: A slot cavity in HL2000. The part was cut before firing; the two halves were realigned after dipping the fired half in solder.

Compared to surface constraint methods, the advantage of HL2000 tape for cavities only increases with the module thickness. Although a surface-constrained part allows significant deformation between the top and bottom layers, the walls of the HL2000 structures remain nearly undistorted since each layer of tape is self-constrained (see Figure 6). This is an important benefit both for control of the cavity geometry and for critical spacing between internal conductor structures.

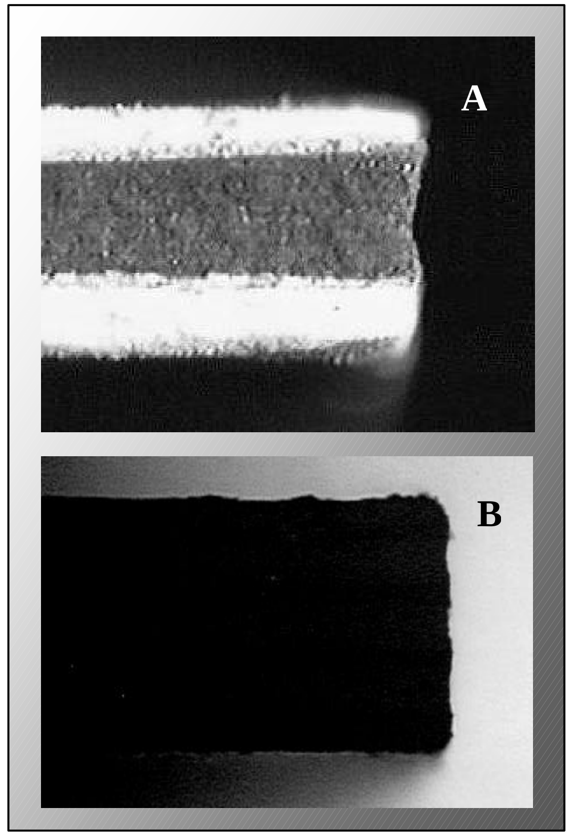

Figure 6: The walls of the surface-constrained LTCC (A) show necking due to the increasing shrinkage of layers further from the edges. In contrast, the walls of the HL2000 tape (B) remain nearly undistorted.

Embedded Passives

The almost ideal performance of the HL2000 tape for cavity structures suggests that non-shrink components with appropriate TCE values can be embedded into HL2000 laminates and fired in place. To illustrate this point, a ferrite transformer has been embedded and fired as shown in Figure 7. Making a direct silver-to-silver contact as shown in Figure 8 has eliminated the need for solder joints and the associated solder-related yield issues. Chip capacitors have been embedded into cavities as shown in Figure 9.

There are benefits for this approach from the standpoint of packaging density and for RF performance. If firing-compatible passive devices can be moved from the top surface of the LTCC module into the body of the module, it frees up space on the outer surfaces of component-limited designs or for laser-trimmed structures. The ability to shield embedded devices with ground-planes may significantly reduce noise and signal cross-talk. Embedded devices may also allow reduced runner length and variation of the placement position relative to other RF structures.

Figure 7: Ferrite transformer embedded in HL2000 before firing.

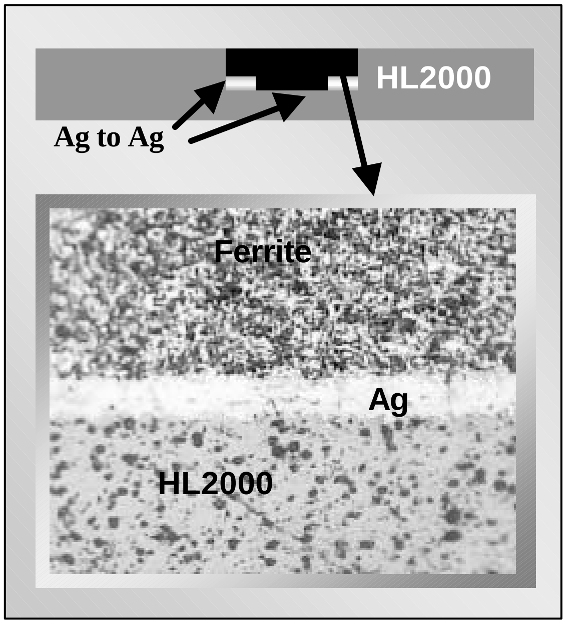

Figure 8: SEM micrograph of silver-silver contact of embedded ferrite structure.

To optimize the usefulness of embedded structures, some changes to the device structure compared to standard SMT configurations may be helpful. Obviously, the presence of the cavity limits routing around the embedded device, so minimizing the height of the devices is more important for these embedded devices than for most SMT applications. Surface routing (or a second tier of components) cannot be accommodated unless the device can be completely buried. To optimize a device for buried embedded applications, a device may also benefit from bottom-side terminations and an organic coating that would burn off and thus allow the buried device to accommodate the z-axis shrinkage of the tape (see Figure 10). A number of other processes associated with tinning and plating of the capacitors can be eliminated for these capacitors.

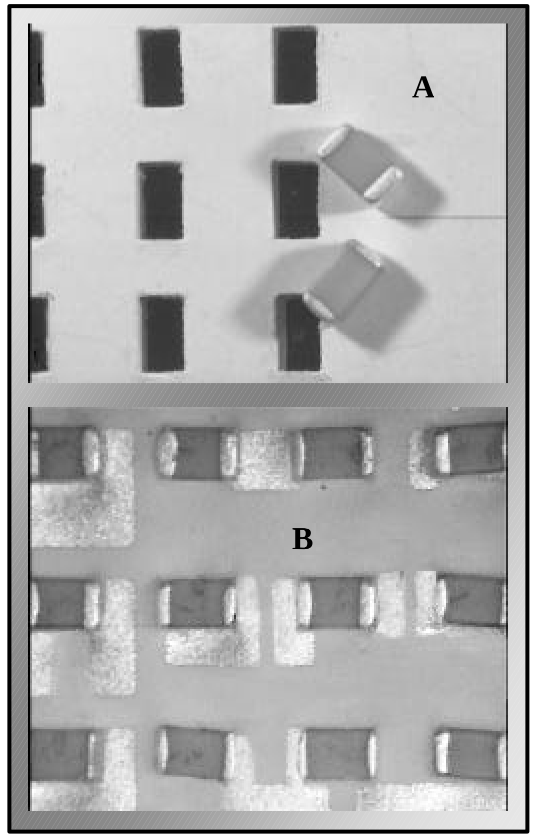

Figure 9: 0603 chip capacitors embedded in HL2000. A: Loose capacitors laying on HL2000 tape prior to lamination. B: Fired structure.

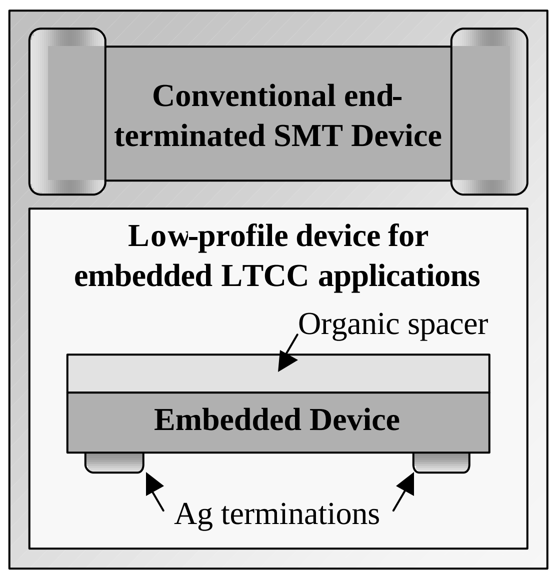

Figure 10: Proposed device configuration for embedded applications.

HL2000 Tape Processing and Effect on Shrinkage

The HL2000 tape is handled using standard free-sintered LTCC processes. The standard isostatic lamination process involves fifteen minutes at 75^{o}C with a laminating pressure of 4500 PSI. The HL2000 firing profile has a burnout zone at about 450 C and a 30 minute peak at a firing temperature of 870 C +/- 10 C.

A discussion of the measurement techniques used to evaluated x-y shrinkage of HL2000 tape laminates during firing can be found in an earlier paper [1]. Table 1 lists shrinkage and shrinkage variations for three casting variations of HL2000 tape made with different organic binder contents and casting parameters. The shrinkage results are shown for both the x and y directions, where the x-axis is in the direction in which the tape is cast and the y-axis is across the width of the tape (see Figure 5).

Table 1: Comparison of x and y shrinkage of three experimental variations V1, V2, & V3 of HL2000.

		X-Y Shrinkage (%)	σ(%)
V1	x	0.107	0.0095
	y	0.121	0.0139
V2	x	0.154	0.0049
	y	0.138	0.0133
V3	x	0.155	0.0062
	y	0.179	0.0060

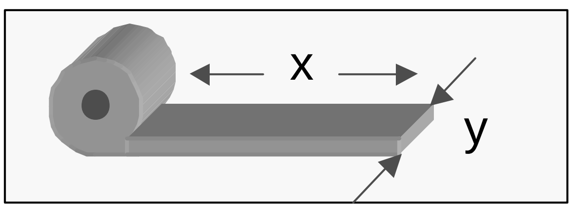

Figure 11: Indicating x and y directions of a roll of tape; x is the length of the tape, y is the width.

How the green HL2000 tape is handled during lamination and between the lamination and firing steps may be more important than firing variations in their effect fired dimensions. For example, an aluminum plate with a TCE of about 25 ppm/^{o}C used during lamination shows a similar length change between room temperature (25ppm/^{o}C x 50^{o} C = 0.125%) as is observed in the laminated tape during firing. This suggests that subtle process variables such as whether or not the plate is warm before bagging, if the part is cooled still sealed and on the plate or removed hot, and cooling time between after lamination and other handling steps, etc., may affect the observed shrinkage.

Because virtually all of the densification of HL2000 occurs in the z-axis, the thickness of the part after firing is a critical measure of the firing profile. An experiment was performed to evaluate the effect of time at peak on the fired laminate shrinkage (FLT). The results, shown in Table 2 indicate that there is no significant change between a firing peak of 30 minutes and 3 hours.

Table 2: Effect of time at peak on z-shrinkage (FLT: Fired Laminate Thickness)

	30 minutes	**180 minutes**
Mean FLT (mils)	14.69	14.71
σ	0.38 %	0.38 %
Z-shrinkage (from laminate)	22.66 %	22.57 %
Z-shrinkage (from loose sheet)	29.36 %	29.27 %

A similar experiment was performed to evaluate the effect of lamination on the fired laminate thickness. In this case, the parts that were laminated once were compared to parts undergoing a second lamination (the double lamination process is often used to prepare test parts); both sets of parts were fired with the now-standard 30-minute peak firing profile. We would expect that the single lamination results would agree with the earlier 30-minute peak results, and the results, shown in Table 3, bear this out. The effect of the second lamination was to slightly reduce the FLT but it also slightly increased the observed variation. As noted before green-handling variations may be a more important source of variations on HeraLock™ shrinkage than firing profile changes. In either case, the thicknesses of the fired laminates are tightly controlled.

Table 3: Effect of single or double lamination on z-shrinkage (FLT: Fired Laminate Thickness)

	Single	**Double**
FLT (mils)	14.63	14.58
σ	0.48 %	0.72 %
Z-shrinkage	29.66 %	29.90 %

Free Surface Glass Effects

A study was performed to evaluate the effects of free surface glass on HeraLock™ HL2000 and on similar, but unconstrained, formulations. The unconstrained tapes were formulated to give a high or low glass content (NC-Low & NC-High, respectively) at the fired tape surface. Evaluation of conductors co-fired on the unconstrained tape showed that the free glass is important for eliminating camber associated with co-fired conductors, but it narrowed the range of formulations that will yield high solderability. The HL2000 has a "dry" glass-free surface that maximizes the solderability of cofired conductors.

The free glass also affects post-fired resistors. To demonstrate this, a resistor formulation intended to give 100 ? /square when post-fired on HL2000 was printed on HL2000 substrates as well as the two unconstrained variations NC-Low and NC-High. Figure 12 shows a graph of the resistor performance on these three surfaces (the resistance values have been normalized to 10 ? thickness). As expected, the resistivity increases with the amount of free glass that can be absorbed during firing.

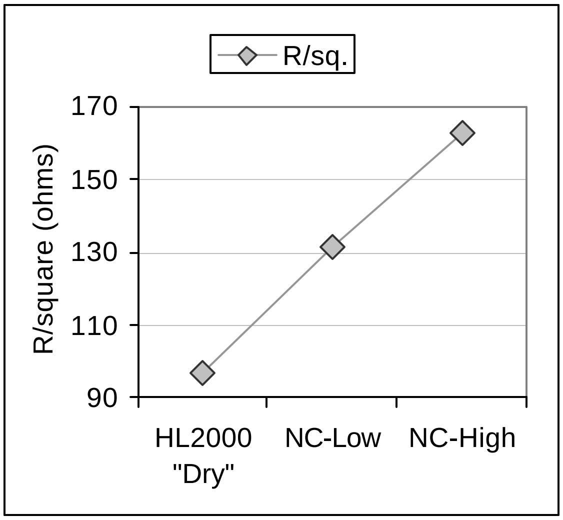

Figure 12: Resistance of a post-fired 100-Ω paste @ 10 μ FFT on printed on tapes with different amounts of free surface glass.

As noted earlier, the advantage of the free surface glass is that it eliminates the camber caused by co-firing conductors with the tape. The solderability-camber scatter graph (Figure 13) suggests that NC-Low formulation makes camber control difficult. The NC-High formulation allowed good control of camber, but some of the experimental cells showed poor solderability. All of the conductors were tightly grouped in the ideal zone when printed on the HL2000 tape.

A sample circuit pattern printed on HL2000 is shown in Figure 14. The top surface has been printed with a solderable AgPt conductor. The bottom surface is printed with a 100% coverage silver ground-plane conductor. On a part with a fired laminate thickness of about 15 mils (0.38 mm), the maximum camber was less than 3 mils (75 ?) over a 2” (51 mm) window. Similar parts made with internal as well as external 100% ground planes have been made with no sign of camber, show-through, or delamination. The ability to design with high-coverage ground planes is important for eliminating the risk of an unwanted resonance associated with the grid geometries [4].

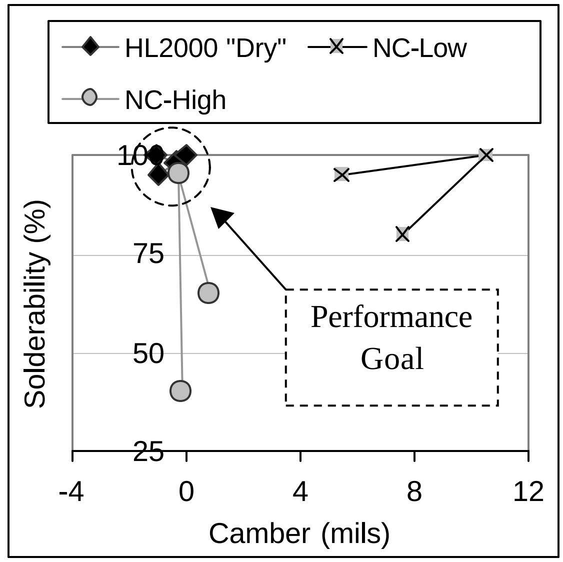

Figure 13: Scatter-plot of solderability versus camber for AgPd conductors printed on tapes with different amounts of free surface glass.

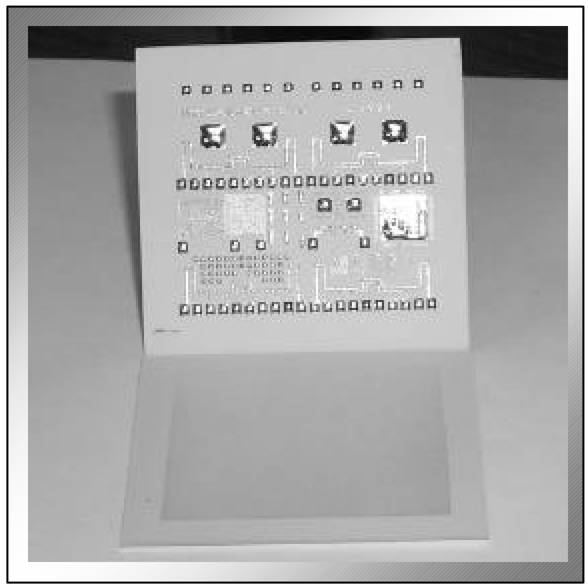

Figure 14: Samples of HL2000 modules. The top of part has been co-fired with AgPt conductor and dipped in 62-36-2 SnPbAg solder. The bottom part is a 100% coverage co-fired silver ground plane.

The rigidity of HeraLock HL2000 that minimizes camber during firing also enables structures to be formed into the tape and fire out with minimal sag or distortion. Figure 15 shows channels that have been formed into a 10 layer HL2000 structure. The channels were formed around Teflon inserts; the inserts were removed after lamination. During lamination the plastic properties of LTCC allows the tape to be conformed to any inserted shape. As long as the insert material doesn’t distort at the lamination temperature and pressure, the self-constraining nature of HL2000 will guarantee for the same shape to be there after sintering.

Figure 15: Channels formed HL2000.

HL2000 Material Set

The following materials have been developed for use on HL2000:

Co-firable Conductor Set
- 99:1 AgPt conductor
- 4:1 AgPd conductor
- Ag routing conductor
- Ag ground plane conductor
- Ag via fill

Post-fired Resistors (TCR < 100 ppm)
- 50 Ω
- 100 Ω
- 250 Ω

Mechanical and RF/Microwave Materials Data

The green HL2000 ?-kit tape has a green thickness of 5.25 +/- 0.2 mils. The green density is 2.3 g/cm^3 and the tensile strength is 240 psi. The fired density is 2.88 +/- 0.04 g/cm^3 and the flexural strength is 250 Mpa. The root mean square fired surface roughness is 0.7 ? m. The thermal coefficient of expansion is 6.1 ppm/^{o}C over the temperature range of 20^{o} to 300^{o} C.

The relative permittivity of fired HL2000 is 7.8 as measured at 2.5 GHZ and at 5.5 GHZ. The dissipation factor was measured at 0.0026 at 2.5 GHz and at 0.0027 at 5.5 GHz. The DC breakdown voltage is greater than 800 volts/layer.

Conclusion

The Heralock™ HL2000 has several benefits for microwave module designs. The HL2000 tape has nearly zero x-y shrinkage (<0.2%) and shrinkage variation (<0.014%) during firing. This control of shrinkage carries over to conductor on the tape, minimizing the distortion of fired RF structures. Low x-y shrinkage enables large format processes that allow reduced manufacturing costs.

Low x-y shrinkage is also valuable for creating precise cavity structures and enables passive devices to be embedded into the tape structure during firing. Direct silver-to-silver terminations avoid the need for solder terminations in these structures. New passive device structures are proposed to maximize the benefits of embedded structures.

The rigidity of the HL2000 tape during firing effectively eliminates camber caused by co-fired conductors. This allows formulating the HL2000 to have minimal surface glass, which, in turn, ensures maximum conductor solderability. High-coverage ground planes can be co-fired on or in the HeraLock™ structure with causing camber or delamination. These solid ground planes give better shielding and can eliminate an unwanted resonance associated with the spacing of grid-structure ground planes.

Acknowledgements

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References

[1] Frans Lautzenhiser & Edmar Amaya, "HeraLock™ 2000 Self-constrained LTCC Tape," Proceedings of the 2002 International Conference on Advanced Packaging and Systems (ICAPS), Reno, Nevada; March 12-13, pp. 143-9, 2002.

[2] Mike Barker & Rick Draudt, "Zero Shrink Process for Cost Sensitive High Volume LTCC Applications," Proceedings of the 2001 International Symposium on Microelectronics (IMAPS), October 9 –11, pp. 26 – 31, 2001.

[3] Edmar Amaya, Peter Barnwell & Frans Lautzenhiser, "Designing with HeraLock™ HL2000 Self-constrained LTCC Tape", Final Program, Advanced Technology Workshop on Ceramic Applications for Microwave and Photonic Packaging, May 2-3, Providence, RI, 2002

[4] S. Shih, A. Becker, Y. Lee & A.M. Lyons, "Design and Characterization of Broadband High Frequency Transmission Lines on Low Loss LTCC," Proceedings of the Ceramic Applications for Microwave and Photonic Packaging, May 2-3, Providence, RI, 2002.