LTCC-based System-in-a-Package Advancements and Market Potential

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Abstract

Research indicates that the packaging markets have come full circle over the past 40 years. In the 1960's, limitations of integrated circuit technology were addressed in part by thick and thin film hybrid technology. At a point in the late 1980's, silicon devices had become significantly easier to bring to market with improvements in performance and density at several orders of magnitude. Thin and thick film technologies lost their technologically competitive edge to the likes of silicon integration and laminate interconnect advancements. In the 1990's, the silicon industry continued to progress at the speed of Moore's Law and technologies such as system-on-a-chip (SoC) emerged. While it is possible to integrate a significant amount of functionality on one silicon device, the cost of doing so may be prohibitive. In some cases, IC's that logically belong together to form a system or subsystem cannot be made on a single die. Packaging technology has advanced to the point where intentionally splitting the system into multiple dice can provide a performance advantage as well as a cost advantage. As in the past, when new technology is introduced, it appears with great fanfare and optimistic market projections. Questions arise regarding the limitations and disadvantages of the new technology and, when inevitably a weakness is identified, other techniques and technologies emerge. One such concept is system-in-a-package (SiP). The use of low temperature co-fired ceramic (LTCC) technology, with its three-dimensional attributes and intrinsic ceramic stability, provides an unequaled solution to high-density packaging of systemic electrical and mechanical structures. LTCC-based SiPs undertake current market potentials in excess of $10B per annum both technically and cost-effectively.

Key words: System-in-a-Package, SiP, System-on-a-Chip, SoC, System-on-a-Package, SoP, LTCC

Introduction

The packaging markets have come full circle over the past half-century. In the 1960's, limitations of integrated circuit technology (limited chip functionality and complexity, inability to realize on-chip high quality and accurate passive elements, mixed signal silicon did not exist) were addressed in part by thick and thin film ceramic technology. These technologies provided the solution to the need for higher integration, mixed technologies and reliability in a package that provided protection and the required I/O (Input/Output). PWB (Printed Wiring Board) technology during this time was lagging the features available to ceramic-based technologies and, bare die and wire bonding to laminate structures had yet to be realized.

Over the next two decades, significant thin and thick film feature improvements occurred less frequently as advances in silicon and PWB technologies. At a point in the late 1980's, silicon devices had become significantly easier to bring to market with improvements in performance and density of several orders of magnitude. Integrated circuit packages had also progressed rapidly, challenging the PWB industry to improve its own feature sets as well (line/space, layer count, via technologies). Thin and thick film ceramic technologies had lost their technologically competitive edge to the likes of silicon integration and laminate interconnect progress.

In response to this, the microcircuit industry devised yet another acronym, a new buzzword, "MCM"

or multi-chip module to describe essentially the exact packaging methods the industry had been using for years. Not to be upstaged, the silicon industry developed MDM-D (deposited substrate) and the PWB industry developed MCM-L (laminate substrate) while the hybrid industry made MCM-C (ceramic substrate). In the end, no one technology dominated and the multi-billion dollar market projections with 40 to 50% CAGR's just never happened.

System-on-a-Chip

In the 1990's, the silicon industry continued to progress at the speed described by Moore's Law and another viable packaging concept, acronym, and buzz word emerged – "SoC" or system-on-a-chip. Expert opinions vary on the actual definition of SoC, but essentially it is meant to describe a "system" contained on a single piece of silicon enabled by a combination of advanced electronic design automation, silicon processing technologies and intellectual property cores and packaging. It is more than an Application Specific Integrated Circuit (ASIC) because it is capable of integrating the processor, ASICs, communications peripherals, DSPs, and analog in a single chip device. This integration of multiple functions results in significant added value. SoC applications feed off multiple markets previously dominated by ASICs, giving it more opportunity for growth [1]. Dataquest recently predicted that SoC designs might comprise up to 55% of the ASIC market [2], while Semico Research predicted that the market would triple to $16B US over a four-year period [3]. This all comes at a price, however, as a typical NRE for a SoC approaches $1M USD – six to eight times that of an ASIC. Driven by this high entry cost, SoC designs typically are targeted at high volume applications led by digital cellular handsets.

While it is possible to integrate a significant amount of functionality in one silicon device, the cost of doing so may be prohibitive. If the increased cost can be justified as in perhaps extremely high volume digital handset applications, then SoC is a viable option. Since the introduction of relatively complex silicon technology, the least expensive path to add functionality to an electronic system was to integrate more on a chip. Today, however, delays for longer on-chip interconnects have begun to have a significant impact on performance. Simply putting circuit elements closer together by placing them on the same die will not necessarily improve signal propagation time.

Further, once the size of the die reaches a certain point (dependant upon the technology and wafer size employed), the yield begins to drop significantly and progressing beyond this point makes little economic sense. The negative effect of this model doomed the 1980's version of the SoC concept, wafer scale integration [4]. Integration aside, there are examples whereby certain portions of a system demand integrated circuits manufactured with different technologies such as GaAs (gallium arsenide) and LDMOS (Laterally Diffused Metal Oxide Semiconductor). Packaging of mixed discrete semiconductor technologies was one of the compelling competencies that launched the hybrid industry years ago. Today, packaging technologies continue to provide the option of splitting a system into multiple dice, expanding performance along with significant cost advantages.

System-in-a-Package

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Broadly speaking, the term SiP describes any packaging solution that 1) uses multiple chips or die, and 2) provides a systemic function as a completed entity (Intel Pentium Processors are in fact, SiP's as they include the processor die and the cache). One may immediately ask what the difference is between SiP and MCM. The answer lies in the cost, the volume potential, and the capability of the interconnect structure to accommodate and process a wide variety of functions and I/O. The MCM market, while still alive, describes high-density substrates for high-performance applications and at high costs (high-end computer and military applications). The other market is for SiPs, also referred to as SoP (System-on-a-Package), which may appear to be a minor play on words, yet the two have significantly different cost and performance models closely tied to the fine distinction between "in" verses "on". Other similar industry terms include MCP (Multi-chip Packages) and FCP (Few-chip Packages). The common baseline for all these terms and techniques is a packaging technology addressing lower cost, higher volume applications (as opposed to higher cost, lower volume MCM applications) and typically using no more than ten die.

All the factors that previously drove packaging solutions from CERDIP to μBGA, from clip-on leads to castellations, from discrete to embedded passives continue to influence the industry today. The consumers' demands for transportability, no-cost reliability, and adaptable products remain omnipresent and as such,

packaging continues to be a significant element in the food chain. Yet in hindsight, individual levels of the food chain met the challenges independently. This paradigm holds together until the system performance or cost targets are no longer met by individual food chain contributors' improvements. For example, on-chip propagation delays are now significantly better than delays introduced by traditional packaging techniques. As well, limitations of RF integrated circuits place large numbers of discrete components on the board making high volume cost targets impossible to achieve.

Packaging has become a significant element in a system or sub-systems' cost-per-function, cost-per-performance. If the "package" provides only the low value-add of the past (mechanical and environmental protection; electrical or optical I/O only), it adds cost and limits performance. For current and future systems, the package must provide higher value-add by addressing performance and cost enhancements with innovative adaptable features that support the system or subsystem part thereof. Ironically, one solution is to simply eliminate the package. Nonetheless, packaging must enter the system at a higher level of assembly. This higher entry point places even greater demands on the packaging technology choice and design to address density and weight, electrical, optical, or fluidic passages, performance, and protection including hermeticity.

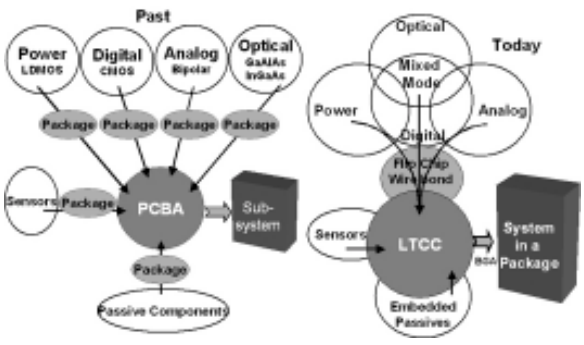

Figure 1. Packaging Trends

LTCC Packaging

Modern packaging must address system requirements beyond the structural role of the past. An ideal package model might attend to some of the following attributes:

- Provide interconnect
- Support multiple assembly techniques
  - Solder (SMD & Flip-Chip)
  - Resin / Epoxy
  - Brazing
  - Welding
  - Eutectic
  - Wire bond
  - Optical alignment
- Support multiple I/O
  - Electrical
  - Mechanical
  - Optical
  - Fluidic
  - Gaseous
  - Waveguide
  - Thermal
- Provide protection
  - Mechanical
  - Environmental
- Integrate circuit components

All of these elements have numerous variants depending on the application. For example, an electrical I/O may need to perform up to 20KHz as an audio connection or it may need to support an optical to electrical signal at 10GHz. The package must impart to the system these copious features while maintaining a profile of stealth; the elements of the system must not be affected or altered by the packaging.

It has been the practice in the PWB and integrated circuit industries to measure densities in terms of in/in^2 or perhaps cm or mm/cm^2 or mm^2. These density figures describe the efficiency of the two-dimensional real estate used to create an integrated circuit or to fabricate a printed wiring board and disregard the key to efficient packaging, the third or "Z" dimension. The notion of a two-dimensional measurement has spawned the term "SoP" or System-on-a-Package. This contrasts with SiP, whereby the package becomes part of the system by providing efficient and innovative use of the Z dimension.

LTCC is a three-dimensional ceramic technology utilizing the Z dimension for interconnect layers, embedded circuit elements, and integral features such as shelves and cavities. LTCC is a mixture of thick film and ceramic technologies. Thick film contributes electrical interconnect and passive circuit elements (resistors, inductors, and capacitors) and ceramic contributes dielectric properties as well as the foundation for physical features from vias to complex stepped cavities and cutouts.

These characteristics allow the designer to 1) effectively use the Z dimension of the system to realize embedded circuitry and interconnect, 2) reuse the X-Y real estate for active and additional passive circuit elements on the top layer, and 3) use the same structure as the package including the required I/O. Further, thick film resistor and capacitor elements may be adjusted by means of YAG-Laser trimming during test allowing precise functions to be realized with less costly, wider tolerance add-on circuit elements. Three-dimensional attributes of a fully utilized LTCC structure are unequaled by any other current affordable technology. This is truly a System-IN-a-Package.

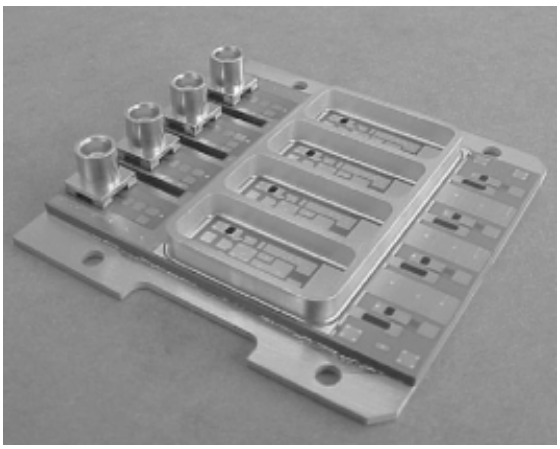

Figure 2c. LTCC Structure

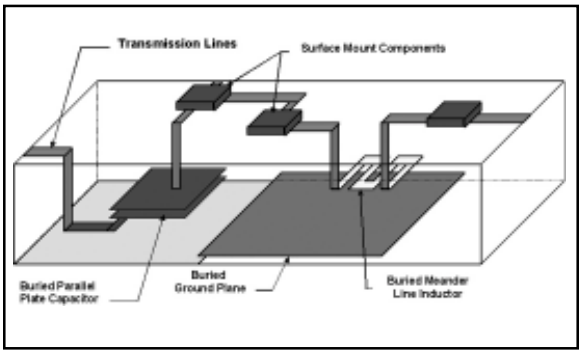

Figure 2a. Embedded RF Features

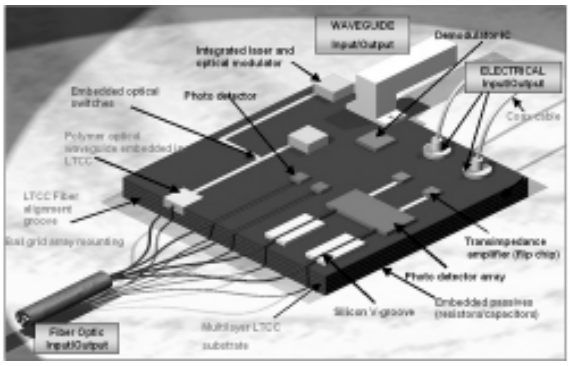

Figure 3. System-in-a-Package [5]

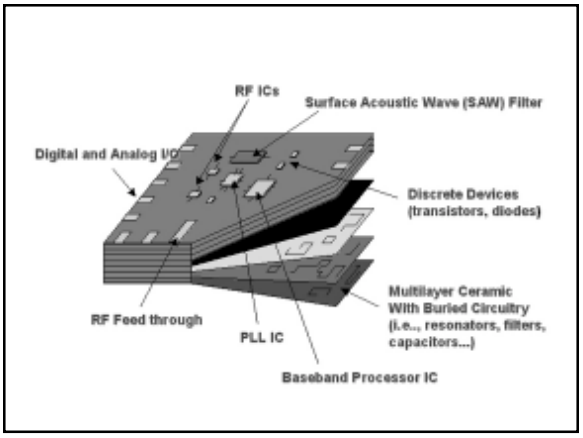

Figure 2b. High-Density Interconnect

The Market

With each cycle of packaging challenges over the past 40 years, two distinct market opportunity paths were available for pursuit.

1. Interim solutions available while long term resolutions are in development (e.g. LTCC Bluetooth ™ package to interconnect a multi-chip system while single-chip solutions are designed and maturized to achieve a $5 price target).

2. Long term packaging solutions that allow silicon revisions, feature changes, cost improvements and volume deployment to occur concurrently (e.g. most prevalent in standard products).

There is no evidence that this trend will not continue with LTCC SiP solutions and therefore, ideally targeted markets and applications would include a mixture of both. Further, consideration of LTCC SiP capabilities and how they differ from other processes, techniques, and technologies pursuing the same is warranted. From a technology and process perspective, two competitive areas emerge: semiconductor integration and laminate interconnect.

Semiconductor integration will continue aggressively toward the ultimate SoC and in fact, will be quite successful addressing certain market segments. Supporting the SoC requirement for very high volumes with the cost and performance benefits realized is the consumer electronics market. SoC will penetrate deeply in applications such as Set-top-Boxes, DVD Players, Digital Televisions, Digital Imaging Devices, Digital Audio Players and Video Game Terminals.

Essentially, semiconductor integration can therefore be considered a benefit to the pursuit of the LTCC SiP market if the applications are targeted at the SoC gaps. LTCC SiP applications can make use of ASIC or SoC integration in providing more and more complex multi-chip solutions. SoC applications still require packaging.

Laminate interconnect, like the semiconductor industry, benefits from an established, broad infrastructure. The technology is widely understood, widely deployed and constantly improved upon to address electrical interconnections. From a competitive technology viewpoint, the ceramic verses laminate comparisons have changed very little. Yesterday's arguments and perceptions form today's differentiators. One can still argue that ceramic increasingly outperforms laminate structures as frequency rises above 1GHz, providing higher Q, lower loss and lower T_f.

Clearly the dominant market opportunity for LTCC SiP applications is communications, which includes Wireless, Optical, and Photonic functions. To a lesser extent, the automotive & industrial markets can be addressed with sensor & MEMS (Micro-Electrical-Mechanical-Systems) applications, followed then by Military/Aerospace potentials.

In recent studies, IMS reported LTCC-based circuits (defined as SMD and chip & wire on LTCC interconnect) have the largest growth potential through 2005 of any category of hybrid circuits and MCMs [6]. In fact, the projected CAGR is 4 to 25 times larger than any other category (thin film, thick film, MCM-D, MCM-L). LTCC-based SiP is capable of addressing a much broader market segment than portrayed in many market studies. Combined with SoC potentials (LTCC SiP as the packaging medium for SoC), MCP and MCM forecasts, the total available market exceeds $15B by 2004. The recent global economic slowdown may postpone actual implementation yet the products and technologies that contribute to the forecast are active and continue to be the focus of the investment communities (optical systems, wireless systems, photonics, automotive electronics, military and aerospace programs).

Conclusion

System-level integration is ideally approached by a combination of integration (SoC) and partitioning (SiP). LTCC-based System-in-a-Package is a cost-effective, adaptable, and scaleable solution to demanding packaging applications. The LTCC infrastructure is well established and is supplying the communications, automotive, and Military/Aerospace markets with high value-ad packaging solutions. Making use of a cubic configuration to integrate the package, the interconnect and passive elements into one structure, LTCC SiP is poised to serve a multi-billion dollar market in the near term and enjoy double-digit CAGRs in the years to come.

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