Thermal Assessment of RF Integrated LTCC Front End Module (FEM)

Victor Adrian Chiriac* **and Tien-Yu Tom Lee**
Final Manufacturing Technology Center
Motorola, Inc.
2100 E. Elliot Road, Mail Drop EL725
Tempe, Arizona 85284
(480) 413-6756* (480) 413-5666
(480) 413-4511 (Fax)
victor.chiriac@motorola.com, tom.lee@motorola.com

ABSTRACT

The thermal performance of Front End Module (FEM) incorporating Low Temperature Co-fired Ceramic (LTCC) substrate is investigated. An Infrared Microscope System was used to measure device surface temperature with both RF and DC power at various duty cycles (25 to 100%). The maximum junction temperature (~112°C) occurs at the second stage. By powering the module with DC only, the comparison between numerical and experimental data indicates good agreement, with less than 10% difference in the peak temperature values.

When replacing the common 2-layer organic substrate with a 14-layer LTCC substrate and silver paste metallization, the peak junction temperature reaches 130.1°C, ~51% higher than before. However, by increasing the silver paste thermal conductivity from 90 to 350 W/mK, a significant drop in peak temperatures occurs, indicating the impact on module's overall thermal performance. The top metal layer thickness (10 vs. 30 microns) only contributed to 5-8% changes in peak junction temperature.

An improved FEM design incorporates a higher thermal conductivity silver paste material (300 W/mK) with new thermal via array structure (25 vias, 150 microns in diameter each) in the LTCC substrate. The module junction temperature reaches 96°C (based on 25°C reference temperature, 100% duty cycle), corresponding to a junction-to-substrate (R_{js}) thermal resistance of 14°C/W. Further study reveals that 20% voiding placed at the die center has no impact on FEM thermal performance, while the voiding placed at the die corner (under the heat dissipating stages) increases the stage peak temperature significantly by more than 40°C.

Last part of the study focuses on design optimization: two particular designs provide the optimal thermal performance when reducing the thermal via number/costs by almost 40%.

NOMENCLATURE

P	Power dissipation (W)
PTH	Plated Through Holes
RF	Radio Frequency
MCM	Multi Chip Modules
PA	Power Amplifier
T	Temperature (K)
t	time (s)
K	Thermal conductivity (W/mK)

INTRODUCTION

Projected increases in interconnect density and requirements for higher clock rates for digital and microwave electronics defined a need in the early 1990 for improvements in traditional microelectronic packaging. The package, together with the interconnect board plus discrete components complicate the assembly, increasing the volume as well as the weight. A new technology could integrate these three functions and reduce the size and assembly complexity with concurrent improvements in cost and reliability.

Requirements for reduced volumes for personal electronic systems for communication are the main drivers for the new technology. Low Temperature Cofired Ceramic is a potential solution for achieving a newly integrated packaging technology from a combination of thick-film and low-temperature co-fired dielectrics [1,2]. It offers a competitive edge in the integrated passive components over other MCM technologies, due to: 1) reduction contacts/transitions number; 2) increased reliability due to less interconnects; 3) cost savings - fewer steps required for component integration, a large number of assembly steps are eliminated; 4) density/space savings - by embedding the components in the substrate layers, the footprint constraints are removed; 5) enhanced electrical performance [3].

This study was initiated with the intent to design, develop and manufacture a state-of-the-art tri band GSM/DCS/PCS Front End Module (FEM) incorporating a novel LTCC technology for application in wireless handsets. The FEM includes the PA, required matching and filtering, Transmit/Receive (T/R) switches, and broadband or dual directional coupler(s). The novelty is represented by the 14-layer ceramic

substrate, replacing the classic 2-layer organic substrate, with positive impact on the module overall size, cost and functionality.

The objective of the study is twofold: 1) to characterize thermally the GaAs PA Front End Module and validate the thermal simulation models ; 2) to predict and optimize the LTCC FEM thermal performance.

COMPARISON BETWEEN ORGANIC AND LTCC MODULES

I. Baseline Organic Substrate Module

A case with organic substrate is considered for comparison purposes. As shown in Fig. 1, the Integrated Circuit (IC) is a 3-stage, dual-band PA placed on a 75 μm thick GaAs die (2.025 x 1.925mm). Six power amplifier MESFET (Metal Semiconductor Field Effect Transistors) stages are placed on the die: 3 for low-band operation and 3 for high-band operation. The low/high-band stages are powered separately. Total power dissipation on the die for low and high-band operation is 5.1 and 4.8 W. Dimensions, power levels and power densities are provided in Table 1. The die contains 80μm diameter solid gold (Au) vias (13 total), connecting MESFETs source pads to backside metallization (plated gold with a total thickness of 3 μm). Gold bond pads (100 x 100 μm size and 25 μm thickness) are located on the die periphery.

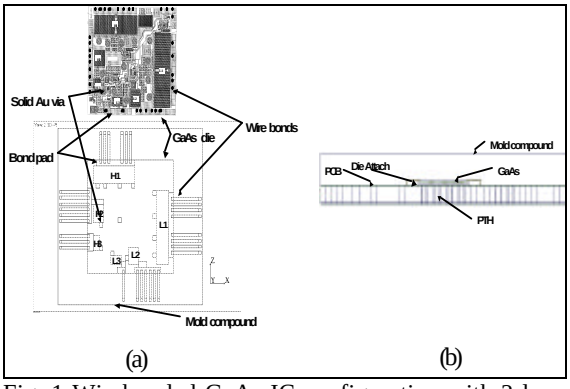


Fig. 1 Wirebonded GaAs IC configuration with 2-layer organic substrate

Table 1 3-Stage Dual-Band Power Amplifier IC

	Stage Dimensions (μm)	Power Dissipation (W)	Power Density (W/mm^2)
L1	300 x 1260	4	10.6
L2	233 x 295	1	14.5
L3	150 x 250	0.1	2.7
H1	300 x 990	3.7	12.5
H2	250 x 300	1	13.3
H3	155 x 250	0.1	2.6

The die is centrally mounted and wire bonded to a 0.5mm thick, 10.5 x 9.5mm, 2-layer organic laminate printed circuit board (PCB). The die attach is a 0.05mm thick SnAg solder. Top and bottom layers are 30μm thick copper metallization. The PCB contains 56 Plated Through Holes (PTHs) vias, 14 located directly under the die, connecting the die pad to the bottom ground plane. The PTHs have 10 mils (0.254 mm) drill diameters, plated with copper thickness of 2 mils (0.05 mm). A dielectric material is used to fill the PTHs. The die and wire bonds are overmolded with encapsulating material for protection.

II. LTCC Substrate Module

The LTCC is an alternative substrate option with 14 metal layers. The substrate core ceramic material has a thermal conductivity of ~3.6 W/mK. The metallic silver paste has initially an estimated thermal conductivity of 90 W/mK. The effective thermal conductivity of the fourteen metal layers is calculated based on the volumetric coverage of the metal in each layer. Table 2 summarizes the values of effective thermal conductivity for different silver paste materials. The top and 7th layers have a thickness of 10 μm, all the others being 5 μm thick. All substrate vias are filled up with the same material as in the metal layers.

III. Numerical Model

The bottom of the substrate is fixed at a constant temperature of 25°C. A previous study indicates that only 4-5% of the total thermal budget is dissipated via natural convection and radiation from this module. Due to this, the model assumes pure conduction with adiabatic boundaries surrounding the module (except the bottom surface). All calculations are based on a 100% duty cycle with only the low-band stages turned on, while all comparisons are based on maximum junction temperature in MESFET stages. A detailed grid study indicates that the grid 87 x 76 x 44 in x, y, respectively z directions captures accurately the physics of the application, yet is not CPU extensive.

In real applications, actual power dissipation ranges usually within 10-50% duty cycle.

Table 2 3-Stage Dual-Band Power Amplifier IC

Metal Layer (L)	% coverage	K^{eff} (K_{metal}=90 W/mK)	K^{eff} (K_{metal}=150 W/mK)	K^{eff} (K_{metal}=250 W/mK)	K^{eff} (K_{metal}=350 W/mK)
L1 (top)	55	51	84.1	139.1	194.1
L2	27.6	27.6	44.3	71.6	99.2
L3	27.6	27.6	44.3	71.6	99.2
L4	27.6	27.6	44.3	71.6	99.2
L5	27.7	27.6	44.3	71.6	99.2
L6	64	58.9	97.4	161.3	225.3
L7	51	47.7	78.3	129.3	180.3
L8	77	70.1	116.3	193.3	270.3
L9	74	67.5	111.9	185.9	259.9
L10	77	70.1	116.3	193.3	270.3
L11	74	67.5	111.9	185.9	259.9
L12	73	66.7	110.5	183.5	256.5
L13	70	64.1	106.1	176.1	246.1
L14 (bottom)	81	73.6	122.2	203.2	284.2

IV. Results and Discussions

Comparisons were based on several design variables: (i) the material in both metal layers and PTH vias, and (ii) the top metal layer thickness. Due to the high temperature co-firing process, the initial thermal conductivity of the silver paste (~90 W/mK) could increase to the property of pure silver (~400 W/mK). Based on this, several metals were examined with thermal conductivity varying from 90 to 350 W/mK (Table 2).

Baseline run indicates that the peak junction temperature with LTCC substrate (with silver paste thermal conductivity ~90W/mK) is 130.1 °C, ~51% higher compared to the baseline case using 2-layer organic substrate with copper metallization, whose peak temperature reached 86.2°C (Fig. 2). By increasing the metal thermal conductivity from 90 to 150, 250 and 350 W/mK, a significant drop in peak temperature occurs. For the case with 350 W/mK, the peak temperature reaches 82.9 °C, 3% lower than the baseline case with 2-layer organic substrate.

In the organic substrate, the top copper layer is 30 µm thick, while in the LTCC substrate the top metal layer is only 10 µm thick. The LTCC substrate top metal layer varied from 10 to 30 µm. Increasing top layer thickness leads to 5-8% decrease in peak temperature vs. the LTCC substrate with 10µm top metal layer. So, the effect of top metal layer thickness is much smaller than the effect of the metal material.

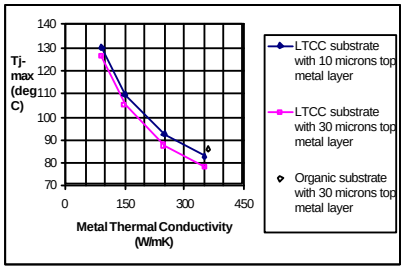


Fig.2 Peak Temperatures vs. Thermal Conductivity

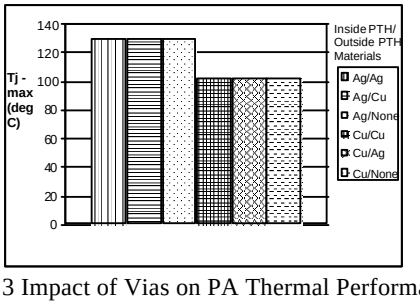


Fig. 3 Impact of Vias on PA Thermal Performance

Next, the impact of PTH vias (under/outside the die) on the package overall thermal performance is investigated. The LTCC substrate has the top metal layer fixed at 10µm and metal layers were silver paste with a thermal conductivity of 90 W/mK. The vias materials are either silver paste (Ag) or copper filled with dielectric material, or without metal. The 14 vias placed under the die provide ~99% of the heat removal from the die through the substrate, while the outer vias did not make a significant impact on the thermal performance (Fig. 3). A large temperature drop (~24%) occurs when the inner PTH vias with silver paste were replaced with Cu. The PTH vias placed under the die make the biggest impacts to the overall thermal performance; same was found when changing the metal layer material from silver paste to K=350 W/mK (approaching pure Cu properties).

EXPERIMENTAL THERMAL MODULE CHARACTERIZATION

I. Experimental Set-up

An experiment is conducted to validate the numerical model. The LTCC module is epoxy mounted onto a 50 mm x 50 mm x 1.1 mm thick 4 layer, 1 oz copper FR4 board (Fig. 4).

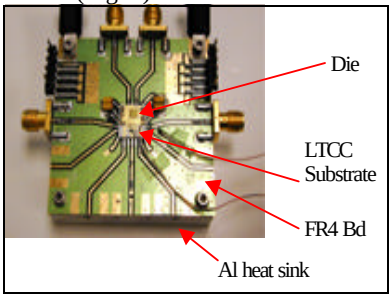


Fig.4 LTCC FEM Module

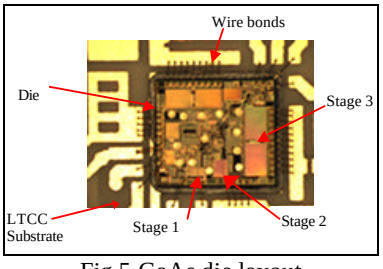


Fig.5 GaAs die layout

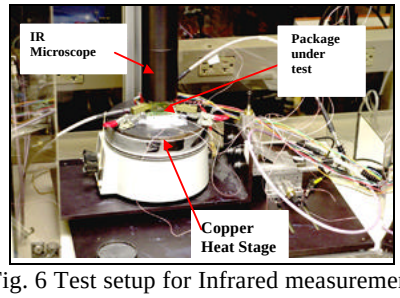


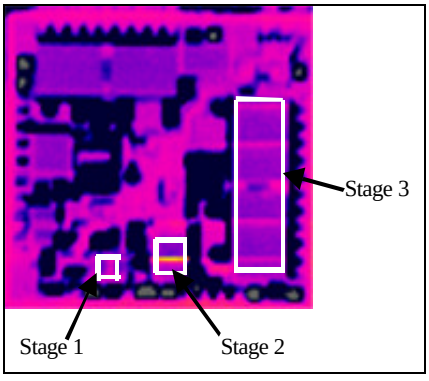
Fig. 6 Test setup for Infrared measurement

The FR4 board has 175 thermal vias 0.4 mm in diameter, mounted onto a 50mm x 50mm x 13mm aluminum heat sink while the tri-band three stage GaAs die is 1.8mm x 2.2mm x 0.1mm, solder mounted onto 8.5mm x 9mm x 0.7mm 14 layer LTCC substrate (Fig. 5). There are 39 gold wire bonds on the die. The gold wire is 0.04 mm in diameter. Stage 3 has the largest finger area, followed by stages 2 and 1.

The test package is clamped on a copper heat stage under the Agema 900 infrared (IR) microscope (Fig. 6). The thermal paste (0.06 mm thick) is spread uniformly between the heat sink and heat stage. Both RF/DC power is applied through a combination of DC power supplies and a RF signal generator. Four thermocouples are used to measure the LTCC, FR4 and heat sink temperatures. One thermocouple is suspended in the air near the IR to measure the ambient temperature, another thermocouple is in the middle of the copper hot plate.

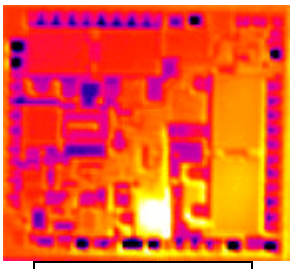
II. Test Procedure

For surface temperature measurement with IR microscope, the emissivity values of the sample surface are needed. The technique with automatic emissivity calculation with reference images is used. The copper heat stage is heated from 60°C in 20°C increments up to 180°C (device is not powered in this process). At each temperature, the thermal image of the device is recorded and stored as a reference image. After all reference images are stored, the package is powered with approximately 36 dbm of RF power and 4.8 watts of DC power.



Temperature Data (°C)	
Stage 1	26
Stage 2	51
Stage 3	27
Ambient	24.6
LTCC	27.1
PC Board	26.2
Case (Al HS)	25.5

Fig.7 12.5% Duty Cycle



Temperature Data (°C)	
Stage 1	70
Stage 2	112
Stage 3	77
Ambient	25.1
LTCC	43.4
PC Board	37.3
Case (Al HS)	32.5
Cu Hot Plate	31.6

Fig.8 100% Duty Cycle

Data is collected at 12.5%, 25%, 50% and 100% duty cycles (DC square wave). The module pulse is 4.6ms; so at 12.5% duty cycle the DC is "powered on" for 575 µs. At each duty cycle, device thermal image is recorded and compared with two reference images; to obtain the true surface temperatures.

The stage temperature data in the tables are the maximum temperatures observed by the IR camera within each stage. Only the 12.5% and 100% duty cycle thermal images are presented here (Figs. 7, 8). For both measurements, the maximum junction temperature occurs at the second stage, and stage 3 is slightly hotter than stage 1. At 100% duty cycle, stage 2 reaches 112°C.

In order to perform simulation validation, separate tests with DC power only were conducted. The measured power dissipations are shown in Table 3 based on 25%, 50% and 100% duty cycles. The IR measured results are shown in Table 4. As seen, under DC power only, the third stage reaches the peak temperatures, identified by the hot spots.

Table 3 Power Dissipation from each Heat Stage (DC)

Location	DC Power Levels		
	25%	50%	100%
Stage 1	0.0125 W	0.025 W	0.05 W
Stage 2	0.0875 W	0.175 W	0.35 W
Stage 3	0.95 W	1.9 W	3.8 W

Table 4 Measured Temperatures at DC Power Only

%power	Temperature measured by thermocouple (°C)					Maximum temp. measured by IR (°C)		
	Amb	LTCC	FR4	Al block	Hot plate	Stage 1	Stage 2	Stage 3
25	24.2	32.6	29.6	27.5	26.9	35	37	55
50	24.2	35.4	30.6	27.9	27.1	48	51	86
100	25.1	47.4	39.2	33.0	32.1	84	93	134

III. Numerical Analysis and Validation

In order to validate the simulations, the entire assembly is modeled, including the LTCC module, FR4 test board, aluminum heat sink and the copper hot plate. The assembly is open to natural convection and radiation environment, except for the bottom of the copper hot plate, fixed at a given temperature. A Computational Fluid Dynamics (CFD) tool Flotherm [4] is applied, solving the conjugate heat transfer problem.

The flow surrounding the assembly is shown in Fig. 9. The thermal plume due to buoyancy occurs above the MESFET stages. The velocity field values indicate a weak airflow circulation in the vicinity of the package. A conjugate conduction-convection case could be replaced by a conduction-case with all package faces insulated except the bottom of the hot plate, fixed at given temperature. A conduction model verifies this, and the temperature difference between the two cases is within 1%.

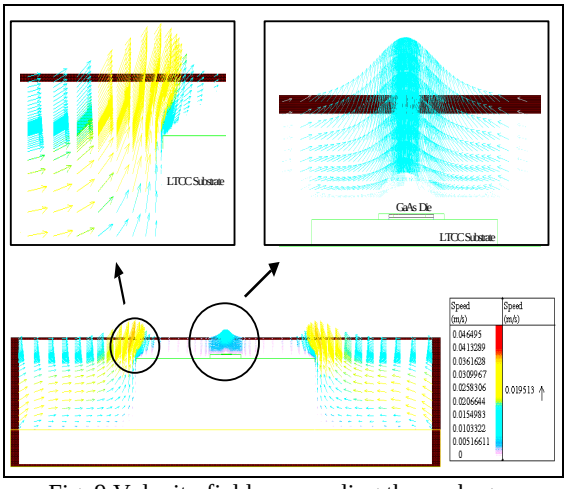


Fig. 9 Velocity field surrounding the package

Comparison between simulation and IR is shown in Table 5; the difference varies from 0.6 up to 14.7%. The average percentage error among the three heat stages is ~8% indicating good agreement between the numerical simulations and IR measurements.

Table 5 Comparison between Simulation and IR Tests

	Power Levels								
	25%			50%				100%	
Location	Peak Temp. °C (Sim)	Peak Temp. °C (IR)	Err. (%) (+) (-)	Peak Temp. °C (Sim)	Peak Temp. °C (IR)	Err. (%) (+) (-)	Peak Temp. °C (Sim)	Peak Temp. °C (IR)	Err. (%) (+) (-)
Stage 1	36.02	35.0	*2.9*	49.2	48	*2.5*	74.8	84	-10.9
Stage 2	40.1	37.0	*8.3*	57.5	51	*12.7*	83.9	93	-9.7
Stage 3	49.79	55.0	-9.5	78.1	86	-9.1	123.9	134	-7.5
LTCC	27.8	32.6	-14.7	32.3	35.4	-8.8	42.4	47.4	-10.5
FR4	25.9	29.6	-12.5	28.4	30.6	-7.2	33.6	39.2	-14.3
Al - Heat Sink	25.7	27.5	-6.6	28.06	27.9	*0.5*	32.8	33.0	-0.6
Cu Hot Plate	25.1	26.9	-6.7	26.2	27.1	-3.3	30.5	32.1	-4.9

The discrepancy is due to: (i) location difference between simulation monitor points and thermocouples; (ii) possible voids in interfaces (simulations assume void free interfaces), and (iii) power density differences between the real and simulated models.

Fig. 10 displays the trend in stage peak temperature variations with increasing duty cycle. The peak temperatures vary almost linearly with increasing duty cycle, as the thermal behavior of the stages is affected mostly by the conduction inside the stack-up. The largest temperature difference between measurement and simulation occurs in the smallest stage (Stage 1), as the power levels vary compared to the simulated values (the simulation assumes 1:7 ratio between Stages 1 and 2).

Another comparison of temperature field based on 100% duty cycle is displayed in Fig. 11. The power density differences between real and simulated conditions may contribute to most of the discrepancy. In the numerical investigation, the power dissipated by each MESFET stage is assumed uniform over the entire area of the stage.

In fact, the stages are composed of many "fingers" dissipating heat; hence the effective area for dissipation is smaller than the entire active area of the stage.

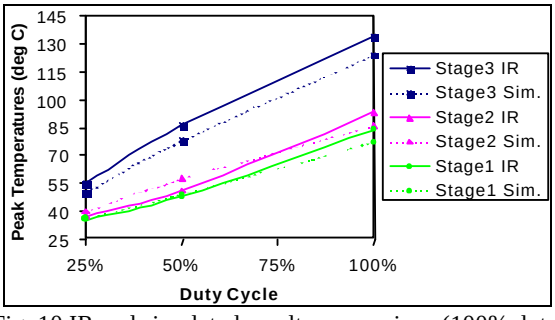
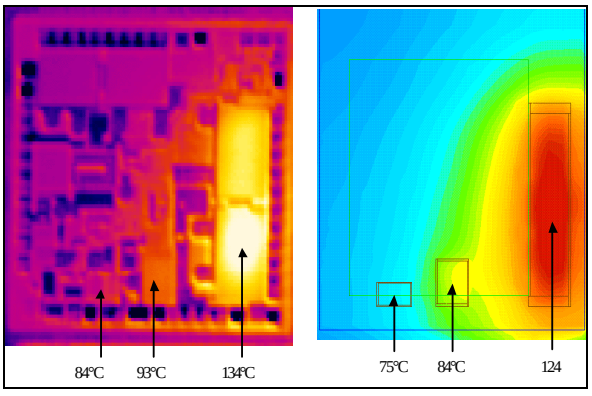


Fig. 10 IR and simulated results comparison (100% duty cycle)

As seen in Fig. 11(a), the hot spot in Stage 3 is actually located in the lower portion of the heat stage regions. Based on this consideration, additional simulations (100% duty cycle) were performed to vary the effective heat dissipation area. By assuming the heat stage region is shrinking to 80% of the original size for each MESFET stage, results (Table 6) show the average percentage error among the three heat stages drops significantly (~6%). This indicates the sensitivity of the power density to the accuracy of numerical prediction.



(a) IRMeasurement (b) Simulation

Fig. 11 Comparison of temperature (100% duty cycle)

Table 6 Comparison on Effective Heat Stage Area

Location	100% Duty Cycle			
	100% Area Coverage		80% Area Coverage	
	Peak Temp. °C (Sim)	Error (%)	Peak Temp. °C (Sim)	Error (%)
Stage 1	74.8	10.9	77.1	8.2
Stage 2	83.9	9.7	86.2	7.3
Stage 3	123.9	7.5	130.1	2.9
LTCC	42.4	10.5	44.8	5.5
FR4	33.6	14.3	35.1	10.4
Al - Heat Sink	32.8	0.6	32.9	0.3
Cu Hot Plate	30.5	4.9	30.6	4.7

OPTIMIZATION STUDY FOR LTCC MODULE

I. Front End Module Design

A preliminary study indicates that the metal silver paste with a thermal conductivity of ~300 W/mK satisfies the thermal requirements of the LTCC FEM module at higher (100%) duty cycles.

Due to the cracks in the core material surrounding the thermal vias during the co-firing process, the thermal via diameter was decreased from 250 µm to 150 µm and the pitch was increased from 350 µm to 400 µm. The number of thermal vias under the die was increased to 25 (Fig. 12). Table 7 summarizes the effective thermal conductivity per layer.

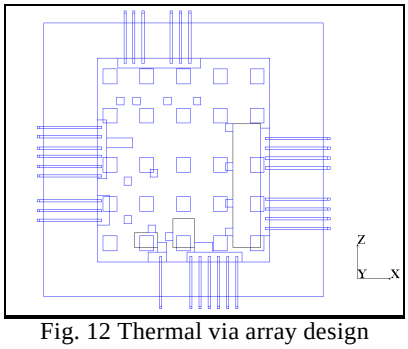


Fig. 12 Thermal via array design

Table 7 Silver Paste Metal Coverage/Effective Layer Thermal Conductivity

Metal Layer (L)	%Ag/%AWG coverage	$K_{eff\text{ - layer}}$ ($K_{silver\ paste}$=300 W/mK)
L1 (top)	70/30	210
L2	15/85	48.06
L3	5/95	18.42
L4	2/98	9.53
L5	4/96	15.46
L6	75/25	225.9
L7	35/65	107.3
L8	83/17	249.6
L9	0/100	3.6
L10	86/14	258.5
L11	0/100	3.6
L12	86/14	258.5
L13	10/90	33.24
L14 (bottom)	90/10	270

II. LTCC Baseline Results

Baseline case indicates that the peak junction temperature of the latest design is ~ 96.5°C at 100% duty cycle (Fig. 13) with the hottest spot located inside the largest MESFET stage. Figs. 14 (a) and (b) show a magnified temperature field in the vicinity of the MESFET stages. There is weak thermal interaction between the stages, as the thermal vias remove heat efficiently from the MESFET stages.

The peak temperature reached by the FEM, based on 25°C substrate temperature corresponds to a junction-to-substrate (R_{js}) thermal resistance of 14°C/W. This value is higher when compared to Rjs = 12°C/W of the FEM module with organic substrate (with 14 thermal vias, 250 microns each). The difference between the two designs is the lower metal coverage provided by the thermal vias placed under the die (14.4% in the new design vs. 22.5% before).

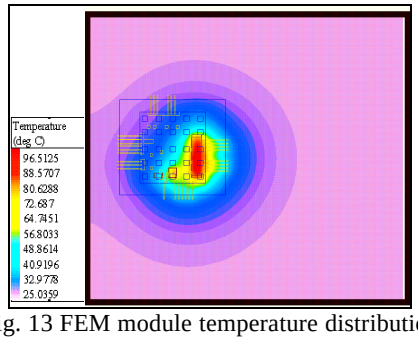
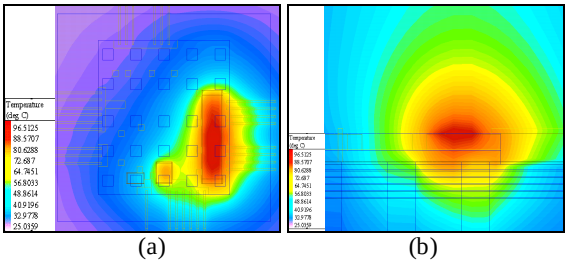


Fig. 13 FEM module temperature distribution



(a) (b)

Fig. 14a, b Top, side views of FEM thermal field

To assess the impact of the thermal via metal coverage on FEM thermal performance, two additional cases were considered: (i) without thermal vias and (ii) with 100% thermal via coverage in the substrate below the GaAs die. The results are summarized in Table 8 and Fig. 15. The peak stage temperature drops significantly below a specific effective thermal via coverage. The higher the metal coverage inside the substrate, the lower the stage peak temperature, due to the enhanced conduction through the substrate. The rate of decay decreases as the metal coverage exceeds a certain value, around 15% (Fig. 15). Beyond this value, the temperature drop is less significant. The design without thermal vias has a peak temperature over 200°C, thus exceeding significantly the allowed thermal budget.

Table 8 Thermal Via metal coverage- sensitivity study

Case No.	Description	Peak Stage Temps (°C)	Thermal Resistance (R_{ja}) (°C/W)
A	No silver paste-filled thermal via	203.3	34.9
B	Current design, 25 thermal vias 150 microns diameter each	96.5	14
C	Old design, 14 thermal vias 250 microns diameter each	88.1	12.3
D	Silver-paste filled thermal via covering 100% the die area	53.1	5.5

III. Impact of Die Attach Voiding on the FEM Thermal Performance

A main concern is the detrimental effect of die attach voiding in higher duty cycle operations. The air volume within the voids increases significantly the thermal resistance across the die attach and device peak temperature. Two cases are investigated: with 20% die attach voiding placed at die center or at die corner, below the heat dissipating stages (Figs. 16a, b).

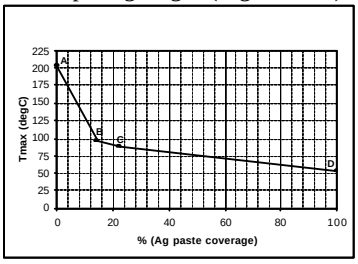


Fig. 15 Temperature vs. metal (Ag) paste coverage

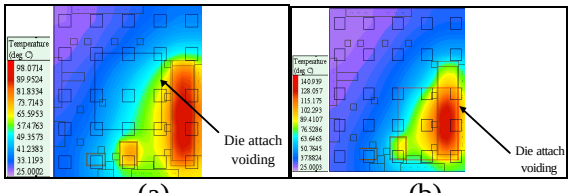


Fig. 16: Temp: (a) central voiding; (b) corner voiding

Two cases with voiding are compared to the void-free case (Fig. 17). The voiding located at die center does not impact the overall thermal behavior. The heat is concentrated in the heat stage areas (Fig. 16a) and conducted through the die attach to the thermal vias. When the die attach voiding is placed at die corner (Fig. 16b), the thermal resistance increases by almost 50%. The voiding acts as an insulator between the heat stages and thermal vias.

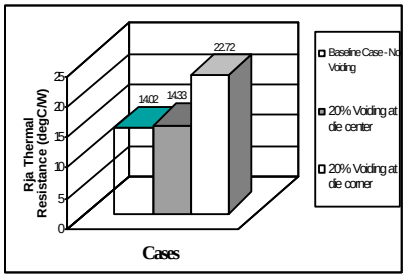


Fig. 17 Thermal resistance comparison between cases with/without die attach voiding

IV. Thermal Vias Design Optimization

The thermal impact of various thermal via layouts is investigated. The purpose is to reduce the manufacturing costs and maintain a reasonable overall FEM module thermal performance. Several design options are shown in Fig. 18. The corresponding thermal fields are summarized in Table 9. The number of vias being removed from the designs range from 4 (Case G) to 15 (Case C).

The peak temperature variation and percentage of thermal vias being removed for each of the investigated cases are shown in Figs. 19 and 20. By removing the same number of thermal vias (9 vias for Cases A and E), the peak temperatures differ significantly, with design E being a preferred alternative. Design F has one more via being removed compared to Design A; however, its peak temperature is 7% lower. Designs A and C are the worst cases since all central vias were removed. It is the location of the removed vias that has decisive impact.

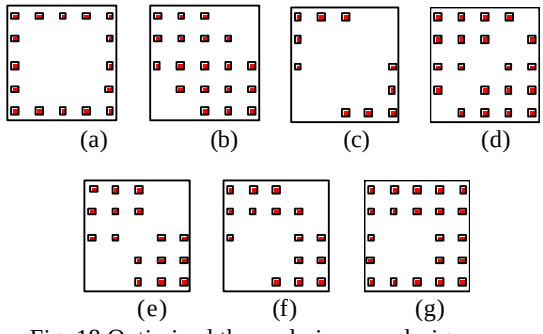


Fig. 18 Optimized thermal via array designs

The optimal combination reduces the number of thermal vias by cutting down the cost, yet maintains the good thermal characteristics of the device. In all of the above design options, Designs E and F are the favorable choices.

Table 9 Junction Temperatures and Thermal Resistances for Various Thermal Via Layouts

Design Types	No. Thermal Vias Removed	Ag coverage in substrate (%)	Junction T_{max} (°C)	R_{js} (°C/W)
A	9	9.3	111.2	16.9
B	6	10.9	99.6	14.6
C	15	5.8	118.7	18.4
D	5	11.6	99.1	14.5
E	9	9.3	102.6	15.2
F	10	8.7	103.2	15.3
G	4	12.1	99.2	14.6

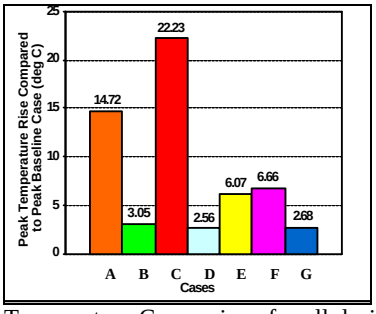


Fig. 19 Temperature Comparison for all designs

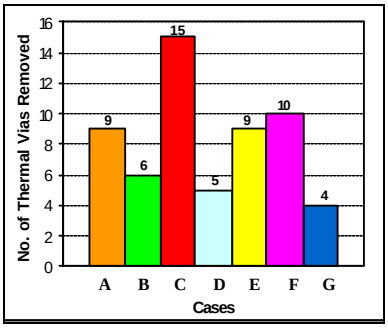


Fig. 20 Summary of cases with removed thermal vias

CONCLUSIONS

The junction temperature for the PA with LTCC substrate and silver paste metallization is 130.1°C, ~51% higher compared to the baseline case with 2-layer organic substrate. Increasing the metal thermal conductivity from 90 (silver paste) to 150, 250, and 350 W/mK, a significant drop in peak temperatures occurs. The thickness of the top metal layer (10 vs. 30 microns) contributes 5-8% changes in peak junction temperature.

The 14 PTH vias placed under the die play an important role in removing heat from the die through the substrate. A test facility and procedure have been developed and the thermal characterization of a LTCC GaAs PA Module using Infrared Microscope was performed. The comparison between the numerical and experimental data indicates good agreement with less than 10% difference in peak temperature values.

The peak temperature reached by the PA with LTCC substrate and silver paste metallization is 96°C (25°C fixed temperature assigned to the substrate's bottom face, 100% duty cycle). This corresponds to a junction-to-substrate (R_{js}) thermal resistance of 14°C/W.

Below a specific thermal via coverage (~15%) the PTH vias placed under the die make the biggest impact on the module overall thermal performance. A 20% die attach voiding placed below the die center has no significant impact on FEM thermal performance. The opposite occurs when the voiding is placed at die corner (under the heat stages), as the temperature increases significantly by more than 40°C.

Last part of the study focuses on the design optimization of thermal via pattern at reducing manufacturing and assembly costs, while maintaining reasonable overall FEM thermal performance. Several options consider a reduction in the number of thermal vias, ranging from 4 to 15 at various locations: two particular designs provide the optimal thermal performance when reducing the thermal via number/costs by almost 40%.

ACKNOWLEDGEMENTS

The authors would like to acknowledge Vern Hause, Mike Hook, Katsumi Kohata, Osamu Izumi for their help with IR measurements and expert assistance, and thanks for the managerial support of Elie Maalouf. Thanks go also to Robert Hapke for maintaining the computer network.

REFERENCES

[1] Tosaka, S., Hoshi, K., Honda, T, "Properties of Low Temperature Cofired Multilayer Ceramic Substrates with Buried Passive Components", Proc. 4-th International Microelectronics Conf., p. 83 - 89, 1988.

[2] Hayashi, H., Ikeda, T., Nishigaki, S., "Newly Developed Multilayer Small Size LC Chip Elements for EMC Noise Filters Made by Low Temperature Fireable Ceramics", International Symposium on Microelectronics, International Society for Hybrid Microelectronics, Orlando, FL., pp.508-512, 1991.

[3] R.L. Keusseyan, "Brazing the Green Tape™ ", Proceedings of the International Symposium on Microelectronics, International Society for Hybrid Microelectronics, Baltimore, pp. 279-286, 1989.

[4] Flotherm, 1999, Version 2.2, Flomerics Ltd., Surrey, England.