Manufacture of Embedded Integrated Passive Components into Low Temperature Co-Fired Ceramic Systems

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Abstract

The next generation of integrated electronic packaging will require higher densities, fewer external interconnects, faster clock rates, lower costs and demand higher reliability. A new emerging technology of embedding integrated passive components (IPC) in Low Temperature Co-fired Ceramics (LTCC) will allow inductor, resistor and capacitor components (RLC) to be placed within the LTCC structure resulting in increased density, reduced interconnects, increased clock speeds, reduced assembly times, thus reducing the package overall cost with increased product reliability. Rockwell Science Center cooperated with Scrantom Engineering, Inc. to test and develop an initial IPC design library.

Key Words: Low Temperature Co-fired Ceramics (LTCC), Integrated Passive Components (IPC), Resistor, Inductor & Capacitor (RLC)

Introduction

The focus of this paper is on characterization of embedded passive components in LTCC structures. Developing IPC design models and then integrating the model out puts into functional designs will be addressed that are required to meet the demands of wireless, high frequency, MCM and high speed digital packaging.

Capacitors (passive)

When designing and establishing manufacturing processes for parallel plate capacitors, specific model parameters need to be identified and implemented. Visual parameters: flatness, local distortion, blistering, discoloration and microstructure. Structural parameters: dielectric/part thickness, proximity to other passives and conductor pad size. Electrical parameters: dielectric constant (k), capacitance (C), dissipation factor (DF), voltage breakdown (V_{BD}), insulation resistance (IR) and temperature coefficient of capacitance (TCC).

SEI set out to develop and manufacture multiple buried capacitors of values ranging to 5000pf with X7R or NPO characteristics. The integrated passive components criteria is, to fire flat with no materials incompatibility and electrically perform consistently as designed using standard silver and gold conductor systems.

Embedded capacitors may be designed using these parameters with the capacitor model relationship after firing being simplified to:

$$C = \frac{(k)(A)(0.2247)}{(t)}$$

Thickness to area relationship being

$$\frac{(t)}{(A)} = \frac{(k)\ (0.2247)}{(C)}$$

Where: A = conductor pad length x conductor pad width, k = dielectric constant of capacitor material, and t = capacitor dielectric thickness.

A software design program for determining capacitor size has been developed and implemented by SEI.

Background

An in depth evaluation of numerous capacitor dielectric materials embedded into the (4) tape systems was performed over the past two (2) years. Each tape system reacts differently to embedded capacitor dielectric material, primarily due to the shrinkage mismatch and LTCC glass migration into the capacitor dielectric. This glass migration also adversely effects the electrical properties, termed "poisoning" which occurs during firing. Low Fire capacitor dielectric materials typically sinter at temperatures 950^0C to 1250^0C, the difficulty arises when firing temperatures drop below 900^0C at which LTCC fires at. Alterations in the capacitor dielectric materials are necessary to attain the electrical performance and desired visual criteria. The alterations consist of modifiers, shifters and sintering agents which are added to the calcined dielectric precursers and blended. This homogeneous blended mixture of dielectric powders and additives are milled to well disperse, prior to creating the dielectric tapes and inks. In this manner high quality factor, low loss dielectric having high K values can be achieved. After careful examination and evaluation of the developed capacitor dielectric materials, candidates were then chosen for the capacitor test coupon to be evaluated for repeatability and electrical characteristics. Over 20,000 capacitors consisting of numerous dielectric compositions have been fabricated for the development, tolerances, repeatability and process establishment of the 1P, 2P and 3P process series.

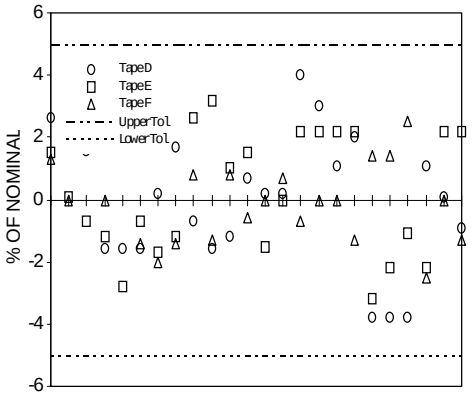
Buried capacitors were fabricated utilizing three (3) processing techniques [1P Process, 2P Process & 3P Process]. 1P process utilizes standard tape system dielectric for the active layer with a maximum conductor pad size of .250 sq.in.. 2P process incorporates tape system matched capacitor dielectric materials in a single layer format with a maximum conductor pad size of .050 sq.in. 2P process also incorporates the thinnest dielectric actives with the highest capacitance per area presently in production. 3P process utilizes a 3-dimensional tape form type processing with a maximum conductor pad size of .100 sq.in, and is less expensive to process than 2P processing. Each process type had capacitors integrated at various layers to determine effects of varying depth. These integrated passive coupons contain twenty-four (24) capacitors of six (6) varied sizes Gold and Silver metalizations were used, this section is confined to the later.

Fired coupons were initially inspected and characterized for flatness, conductor/dielectric compatibility and other various visual defects.
Electrical testing of capacitors was performed on an HP 4262A LCR meter with a coaxial test probe fixture to minimize stray capacitance. The majority of capacitance and DF testing was measured at a frequency of 10kHz. Due to materials compatibility and shrinkage mismatch, one of the LTCC systems was omitted from the TCC, tolerance, CAP/DF data analysis in this section. The compatibility complication leads to visual failure between the buried capacitor materials and the LTCC tape system during 2P and 3P processing. The materials compatibility problem is presently being corrected.

Results

Capacitors utilizing 1P Process exhibit NPO characteristics for k, DF, V_{BD} and the TCC has a slightly positive temperature and frequency dependence (see TCC figures 2 & 3). Tolerances of ±5% ("J") are reproducible for capacitance values from 5pf to 50pf (see capacitance/DF tolerance figure 1).

Figure 1



1P process had insulation resistance typically greater than 10^{10} ohms with the highest break down voltage, exceeding 1000V.

Figure 2

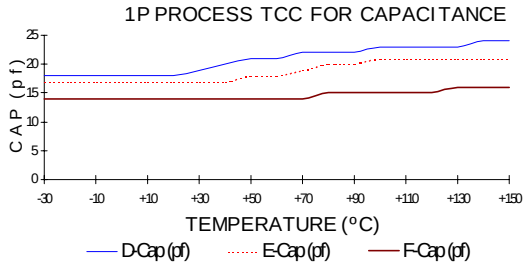
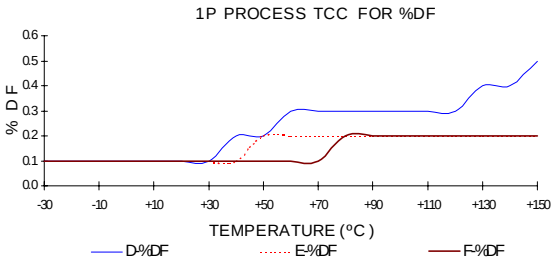
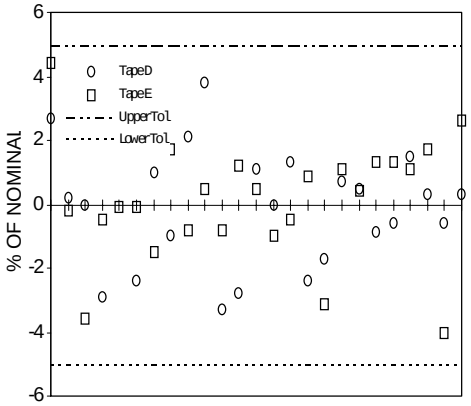


Figure 3



Capacitors utilizing 2P Process exhibit X7R characteristics (see TCC figures 5 & 6). Tolerance of ±10% ("K") are reproducible for capacitance values ranging from 100pf to 5000pf. (see capacitance/DF tolerance figure 4).

Figure 4



Break down voltage is typically greater than 500V for the 2P process.

Figure 5

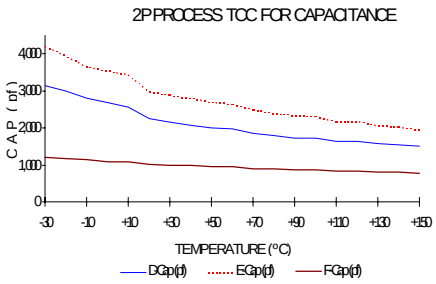
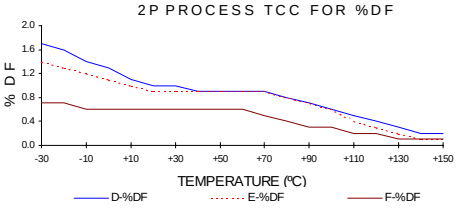
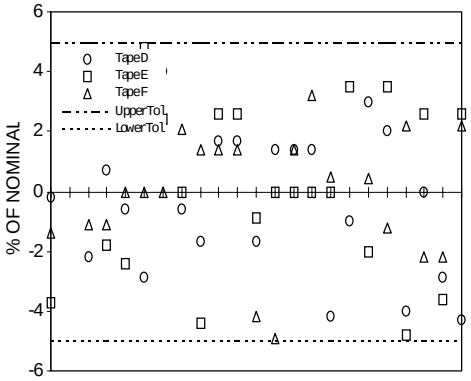


Figure 6



Capacitors utilizing 3P Process exhibit X7R characteristics (see TCC figures 8 & 9). Tolerances of ±10% ("K") or better are typical for this type of processing with Capacitance values range from 10pf to 100pf (see capacitance/DF tolerance figure 7).

Figure 7



V_{BD} measurements in all coupons tested exceeded 700V and no failures from shorts.

Figure 8

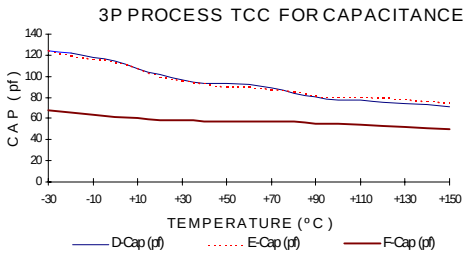
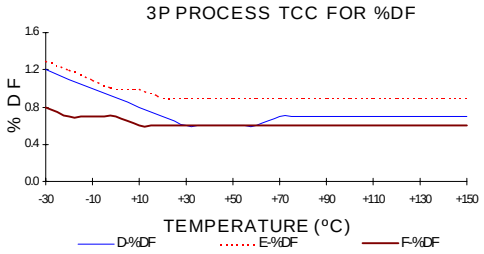


Figure 9



No statistical variation in capacitance or DF was observed while varying the capacitor depth in the coupon

On Target Resistors

The ability to use both surface and buried co-fired resistors in a design is an essential element to the Integrated Passive Component (IPC) concept. Resistor placement is sometimes critical to the performance of RC, LRC, microwave power divider or filter networks. For each case there is a trend towards tighter resistor tolerances, hence the need to identify both materials and processes that produce " On Target Resistors ".

Background

During the early stages of LTCC development (1988-1994) control of buried resistor values was reported to be marginal and tolerances of ± 40% - 50% were not uncommon. As tape and resistor compositions were continually being modified during this time frame (along with just in time process modifications) this should not come as a complete surprise to those who have followed LTCC's development. While this loosely toleranced methodology was grudgingly accepted by microwave engineers at the time, at lower frequencies 7-10 GHz, its hardly adequate at today's operating frequency ranges of 30 - 40 GHz. Today, most electrical engineers prefer buried resistor tolerances of ± 1% - 5% and would probably be grateful to get ± 10% - 20%. While 1% - 5% is still a goal, 10% - 20% is a reality if proper design considerations are followed and one exercises intelligent control of their processes. In fact, at the time of this writing, product fabricated in production runs, using internal design guidelines, has been produced exhibiting average resistor values within **3% - 5%** of design (Figure 10) and CV's of **± 7% - 8%** (Figure 11).

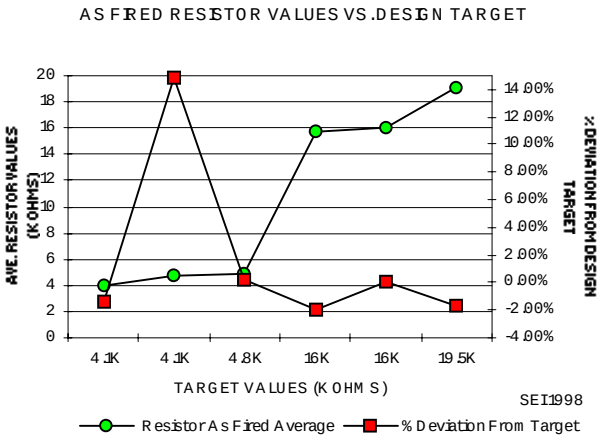
L-18 Taguchi

In the 1995-1996 time frame SEI was engaged in the fabrication of product employing 4 buried sheet values and 3 surface sheet values. Yields were unpredictable and methods to improve yields were sought. In 1996 ITT Corp. agreed to participate and help design an L18 Tagauchi DOE with SEI to identify process and material variables that drive resistor end values and tolerances.

This test matrix was designed to evaluate the effects of resistor aspect ratio, conductor type, lamination - time - temperature - pressure, firing profiles, printed thickness, resistor termination overlap and printing screen mesh sizes on final resistor values and tolerances.

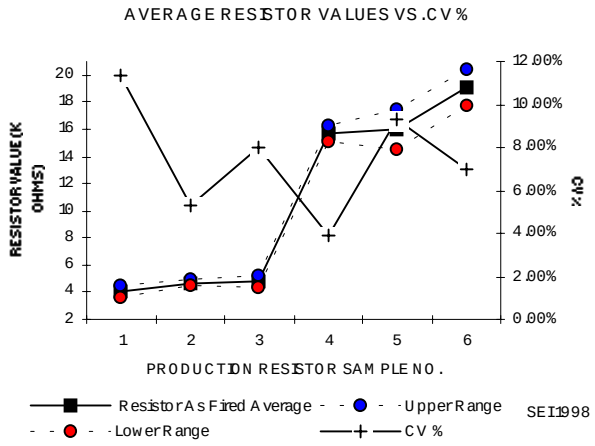
On Target Resistors

Figure 10



On Target Resistors

Figure 11



Results Of The L-18 Taguchi:

1. An optimum screen mesh was identified that produced the most uniform dried thickness (resulting in tighter resistor value distributions) (Figure 12).
2. Resistor yields are highly dependent upon resistor to conductor overlap. While less overlap may be employed, one should expect to experience lower yields.
3. Buried and surface resistor values are predictable on both silver and gold conductors with changes in aspect ratio if lamination and firing profiles are held constant (Figure 13).
4. Lamination time, temperature, pressure and firing profiles are all independent variables. To properly control resistor end values these variables must be fixed during final fabrication.
5. Lamination temperatures above 75°C should be avoided as a trend towards a greater number of electrical opens was noted, especially with minimum resistor/conductor overlaps.

The results of this test may not be overly surprising to those experienced in LTCC resistor processing but certainly lead to the inevitable conclusion as to how closer to target resistor values and tighter distributions may be obtained.

Resistor Design And Process Considerations

Both surface and buried resistors may be designed using the following simplified relationship:

$$R = \frac{\rho\,(l/w) + R_t}{t}$$

Where: **R** = designed resistor value, **ρ** = resistivity of the resistor ink, **l** = resistor length, **w** = resistor width, $\mathbf{R_t}$ = termination resistance and **t** = resistor thickness.

On Target Resistors

Figure 12

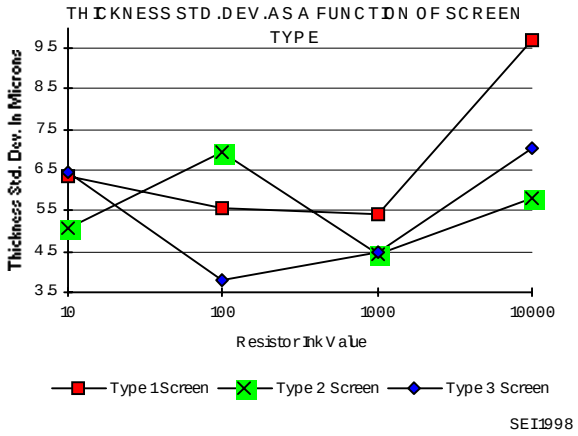
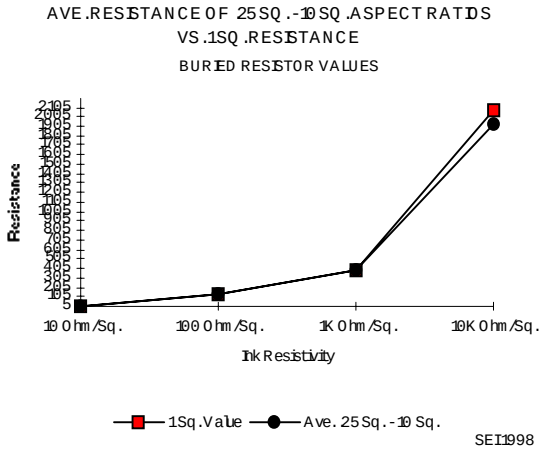


Figure 13



This relationship may be further simplified to **R = ρ (l/w)** by controlling printed thickness and prior in house evaluation of gold / silver interactions with resistor compositions. The final resistor value may be further predicted by blending resistor inks thus eliminating out of bottle variations in resistivity values **(ρ),** in conjunction with LTCC glass interactions and resistor size **(l/w)** due to processing variables such as lamination and firing profiles.

Precision Resistors
Resistor values may be adjusted to tigher tolerances using the following techniques.

Laser trimming
Laser trimming is by far the most popular method of adjusting resistors to value. Tolerances of 1%-2% are obtainable on LTCC by controlling power, cut rate and the number of passes. This method of adjustment most readily lends itself to surface resistors, but may be employed with buried resistors if trim windows are provided in the design.

Electrostatic discharge
Electrostatic discharge is an old technique used to shift resistor values. While this method will adjust resistance values, it is not as repeatable as thermal bumping and may be inconsistent with different resistor lots. In conclusion resistors may be designed using the relationship **R = ρ (l/w)** by proper incoming evaluation of resistor inks, resistor ink blending and control of lamination and firing schedules. Tolerances of 1% - 2% may be obtained using laser trimming.

Inductors (passive)

As wireless systems become more popular and their applications grow, the advantages of high Q (quality factor) components become more apparent. Inductors are often used for matching and in resonant high impedance loads. Although they are an important part in many RF (radio frequency) systems, their performance on substrates such as silicon has been limited thus bounding the overall systems. Larger Q's can be obtained with the use of off chip inductors. This approach does come at the cost of introducing large parasitics that exist between the chip and the inductor.

Inductors implemented in LTCC can achieve values of Q which are an order of magnitude higher than what is typically capable in silicon technology. The power required in higher Q resonant loads is decreased with the square of Q while selectivity is increased. Noise in circuits such as LNA's and VCO's is decreased as Q is increased. Active circuits in the form of die can be recessed in a cavity next to the inductor on the LTCC substrate. This MCM packaging approach minimizes bonding wire lengths and thus decreases the parasitics incurred from going off chip. The high isolation of the ceramic substrate minimizes the unwanted coupling between the inductor and other components.

LTCC technology offers multiple tape layers and interconnecting metals. Test structures were made using FERRO A6, DUPONT 951, HERAEUS CT700 and EMCA T8800. Each of these tape materials were evaluated in both gold and silver. The test coupon contained inductors of the following architecture: square spirals, stacked spirals, circular spirals and torroids. The spiral inductors are varied in their number of turns, trace width, trace spacing and center to first inner turn distance. The torroids are varied in their number of turns and width.

The layout of a square and circular spiral inductor can be seen in Figure 14.

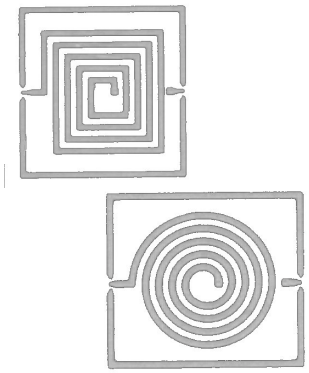
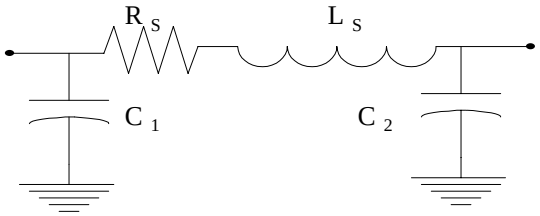


Figure 14: Square and Circular Spiral Inductors

The inductor is probed as a two port with a ground signal ground configuration. The inductors are diced and individually placed in a Wiltron 3680 test fixture. Measurements are

Figure 15: Pi Inductor Model



made with an HP 8753D network analyzer which produces the inductors S-parameters (Scattering parameters). The S-parameters are then manipulated [1] in Mathcad to construct a pi model equivalent of the inductor. This model is shown in Figure 15. Derivations of these components as well as the inductors SRF (self-resonant frequency) and Q are shown in equations 1-5.

$$L_S = \frac{\mathrm{Im}[\frac{-1}{Y_{21}}]}{\omega} \qquad \textbf{eq: 1}$$

$$R_S = \mathrm{Re}[H_{11}] \quad at\ low\ frequency \qquad \textbf{eq: 2}$$

$$C_1 \approx C_2 = -(2\omega * \mathrm{Im}[Z_{11}])^{-1} \quad at\ low\ frequency \qquad \textbf{eq: 3}$$

$$SRF \quad \mathrm{Im}[Y_{11}(f_{SR})] = 0 \qquad \textbf{eq: 4}$$

$$Q = \frac{|\mathrm{Im}[Y_{11}]|}{\mathrm{Re}[Y_{11}]} \qquad \textbf{eq:5}$$

The expected results for the square spiral inductors and circular inductors are calculated [2], [3]. Expected and measured results are shown for square spirals in Tables 2A & 2B using the D system tape with gold traces.

Table 2A

INDUCTOR TYPE	INDUCTOR DIMENTIONS w-width of trace s-spacing of trace n-# of turns	IND. (expected)	IND@ 100 MHz (measured)
Sq. spiral 1	W-10 S-10 N-2.5	19 nH	14.4 nH
Sq. spiral 2	W-10 S-10 N-3.5	40 nH	33.1 nH
Sq. spiral 3	W-10 S-10 N-5.5	122 nH	102.3 nH
Sq. spiral 4	W-10 S-10 N-6.5	186 nH	159.9 nH
Sq. spiral 5	W-10 S-10 N-7.5	270 nH	227.6 nH

Table 2B

IND. TYPE	Q @ 100 MHz (meas.)	Q @ 900 MHz (meas.)	SRF (GHz)	RDC (ohms)	Length on one side (mils)
1	TBD*	TBD*	2.51	0.15	130
2	TBD*	TBD*	1.32	0.4	170
3	TBD*	-	0.546	1.25	330
4	TBD*	-	0.381	1.75	370
5	TBD*	-	0.291	2.2	410

* Test data not available at the time of publication.

Figure 16 shows inductance vs. frequency for the inductors described in Table 2. It can be seen that the inductance is relatively flat over its useful frequency range. The trade off between desired inductance and SRF (self-resonant frequency) is shown in Figure 17.

The SRF is the frequency at which the inductor will begin to resonate by itself. The Q of the inductor will peak at some frequency and begin to decrease up to the SRF at which it will be zero.

Figure 16: Inductance vs. Frequency

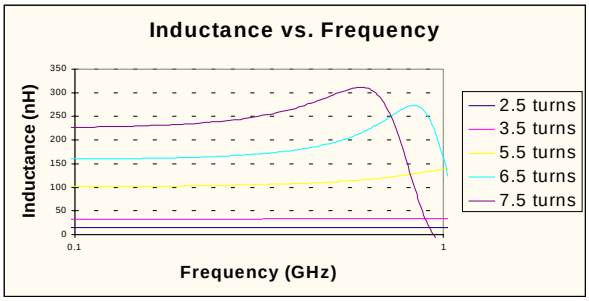
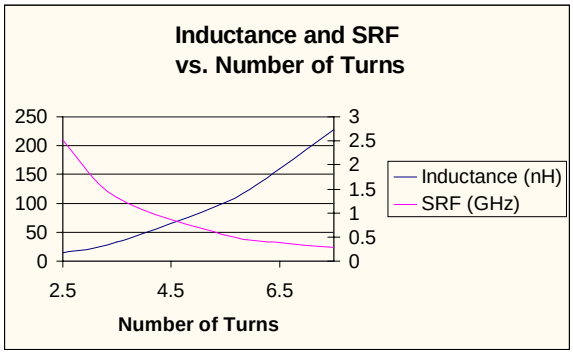


Figure 17:Inductance, SRF vs. # of Turns



A wide range of inductor properties has been shown. The availability of thick metal lines and a highly insulating substrate makes high Q inductors achievable. Multiple inductors can be stacked and isolated with ground planes to increase the area efficiency and overall systems form factor. LTCC offers the ability to recess active die in cavities and embed passives between layers. Impedance's between passives on LTCC as well as isolation between components can be controlled by the designer's layout strategy. When considering these properties of LTCC and how they apply to the needs of many wireless systems, the attractiveness of LTCC can be seen.

Conclusion

It has been demonstrated that LTCC integrated passive component packages maybe manufactured through the use of a design library.

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Bruce Romenesko. Ph.D. Principal Staff Physicist
John Hopkins University. Applied Physics Laboratory

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